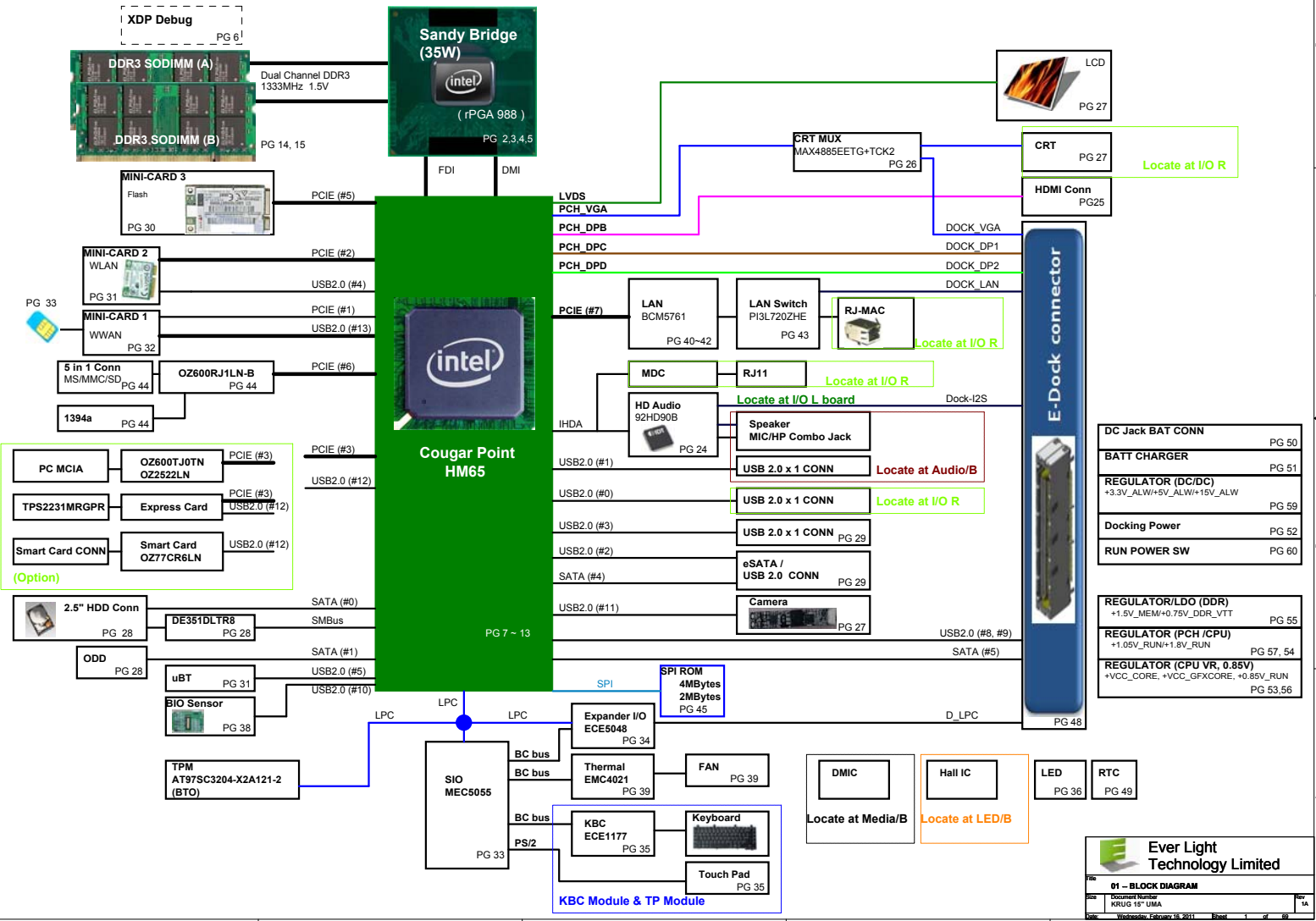
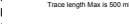


KRUG 15" UMA Block Diagram





DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

CPU SOCKET

DDR_A_CLK0 (16) **DDR_A_CLK1** (16) **DDR_A_CLK2** (16) **DDR_A_CLK3** (16)

DDR_B_CLK0 (16) **DDR_B_CLK1** (16) **DDR_B_CLK2** (16) **DDR_B_CLK3** (16)

DDR_A_CS0 (16) **DDR_A_CS1** (16) **DDR_A_CS2** (16) **DDR_A_CS3** (16)

DDR_B_CS0 (16) **DDR_B_CS1** (16) **DDR_B_CS2** (16) **DDR_B_CS3** (16)

DDR_A_DQ0 (16) **DDR_A_DQ1** (16) **DDR_A_DQ2** (16) **DDR_A_DQ3** (16)

DDR_B_DQ0 (16) **DDR_B_DQ1** (16) **DDR_B_DQ2** (16) **DDR_B_DQ3** (16)

DDR_A_WE0 (16) **DDR_A_WE1** (16) **DDR_A_WE2** (16) **DDR_A_WE3** (16)

DDR_B_WE0 (16) **DDR_B_WE1** (16) **DDR_B_WE2** (16) **DDR_B_WE3** (16)

DDR_A_CMD0 (16) **DDR_A_CMD1** (16) **DDR_A_CMD2** (16) **DDR_A_CMD3** (16)

DDR_B_CMD0 (16) **DDR_B_CMD1** (16) **DDR_B_CMD2** (16) **DDR_B_CMD3** (16)

DDR_A_ODT0 (16) **DDR_A_ODT1** (16) **DDR_A_ODT2** (16) **DDR_A_ODT3** (16)

DDR_B_ODT0 (16) **DDR_B_ODT1** (16) **DDR_B_ODT2** (16) **DDR_B_ODT3** (16)

DDR_A_VREF (16) **DDR_A_VREF1** (16) **DDR_A_VREF2** (16) **DDR_A_VREF3** (16)

DDR_B_VREF (16) **DDR_B_VREF1** (16) **DDR_B_VREF2** (16) **DDR_B_VREF3** (16)

DDR_A_P0 (16) **DDR_A_P1** (16) **DDR_A_P2** (16) **DDR_A_P3** (16)

DDR_B_P0 (16) **DDR_B_P1** (16) **DDR_B_P2** (16) **DDR_B_P3** (16)

DDR_A_P4 (16) **DDR_A_P5** (16) **DDR_A_P6** (16) **DDR_A_P7** (16)

DDR_B_P4 (16) **DDR_B_P5** (16) **DDR_B_P6** (16) **DDR_B_P7** (16)

DDR_A_P8 (16) **DDR_A_P9** (16) **DDR_A_P10** (16) **DDR_A_P11** (16)

DDR_B_P8 (16) **DDR_B_P9** (16) **DDR_B_P10** (16) **DDR_B_P11** (16)

DDR_A_P12 (16) **DDR_A_P13** (16) **DDR_A_P14** (16) **DDR_A_P15** (16)

DDR_B_P12 (16) **DDR_B_P13** (16) **DDR_B_P14** (16) **DDR_B_P15** (16)

DDR_A_P16 (16) **DDR_A_P17** (16) **DDR_A_P18** (16) **DDR_A_P19** (16)

DDR_B_P16 (16) **DDR_B_P17** (16) **DDR_B_P18** (16) **DDR_B_P19** (16)

DDR_A_P20 (16) **DDR_A_P21** (16) **DDR_A_P22** (16) **DDR_A_P23** (16)

DDR_B_P20 (16) **DDR_B_P21** (16) **DDR_B_P22** (16) **DDR_B_P23** (16)

DDR_A_P24 (16) **DDR_A_P25** (16) **DDR_A_P26** (16) **DDR_A_P27** (16)

DDR_B_P24 (16) **DDR_B_P25** (16) **DDR_B_P26** (16) **DDR_B_P27** (16)

DDR_A_P28 (16) **DDR_A_P29** (16) **DDR_A_P30** (16) **DDR_A_P31** (16)

DDR_B_P28 (16) **DDR_B_P29** (16) **DDR_B_P30** (16) **DDR_B_P31** (16)

DDR_A_P32 (16) **DDR_A_P33** (16) **DDR_A_P34** (16) **DDR_A_P35** (16)

DDR_B_P32 (16) **DDR_B_P33** (16) **DDR_B_P34** (16) **DDR_B_P35** (16)

DDR_A_P36 (16) **DDR_A_P37** (16) **DDR_A_P38** (16) **DDR_A_P39** (16)

DDR_B_P36 (16) **DDR_B_P37** (16) **DDR_B_P38** (16) **DDR_B_P39** (16)

DDR_A_P40 (16) **DDR_A_P41** (16) **DDR_A_P42** (16) **DDR_A_P43** (16)

DDR_B_P40 (16) **DDR_B_P41** (16) **DDR_B_P42** (16) **DDR_B_P43** (16)

DDR_A_P44 (16) **DDR_A_P45** (16) **DDR_A_P46** (16) **DDR_A_P47** (16)

DDR_B_P44 (16) **DDR_B_P45** (16) **DDR_B_P46** (16) **DDR_B_P47** (16)

DDR_A_P48 (16) **DDR_A_P49** (16) **DDR_A_P50** (16) **DDR_A_P51** (16)

DDR_B_P48 (16) **DDR_B_P49** (16) **DDR_B_P50** (16) **DDR_B_P51** (16)

DDR_A_P52 (16) **DDR_A_P53** (16) **DDR_A_P54** (16) **DDR_A_P55** (16)

DDR_B_P52 (16) **DDR_B_P53** (16) **DDR_B_P54** (16) **DDR_B_P55** (16)

DDR_A_P56 (16) **DDR_A_P57** (16) **DDR_A_P58** (16) **DDR_A_P59** (16)

DDR_B_P56 (16) **DDR_B_P57** (16) **DDR_B_P58** (16) **DDR_B_P59** (16)

DDR_A_P60 (16) **DDR_A_P61** (16) **DDR_A_P62** (16) **DDR_A_P63** (16)

DDR_B_P60 (16) **DDR_B_P61** (16) **DDR_B_P62** (16) **DDR_B_P63** (16)

DDR_A_P64 (16) **DDR_A_P65** (16) **DDR_A_P66** (16) **DDR_A_P67** (16)

DDR_B_P64 (16) **DDR_B_P65** (16) **DDR_B_P66** (16) **DDR_B_P67** (16)

DDR_A_P68 (16) **DDR_A_P69** (16) **DDR_A_P70** (16) **DDR_A_P71** (16)

DDR_B_P68 (16) **DDR_B_P69** (16) **DDR_B_P70** (16) **DDR_B_P71** (16)

DDR_A_P72 (16) **DDR_A_P73** (16) **DDR_A_P74** (16) **DDR_A_P75** (16)

DDR_B_P72 (16) **DDR_B_P73** (16) **DDR_B_P74** (16) **DDR_B_P75** (16)

DDR_A_P76 (16) **DDR_A_P77** (16) **DDR_A_P78** (16) **DDR_A_P79** (16)

DDR_B_P76 (16) **DDR_B_P77** (16) **DDR_B_P78** (16) **DDR_B_P79** (16)

DDR_A_P80 (16) **DDR_A_P81** (16) **DDR_A_P82** (16) **DDR_A_P83** (16)

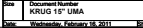
DDR_B_P80 (16) **DDR_B_P81** (16) **DDR_B_P82** (16) **DDR_B_P83** (16)

DDR_A_P84 (16) **DDR_A_P85** (16) **DDR_A_P86** (16) **DDR_A_P87** (16)

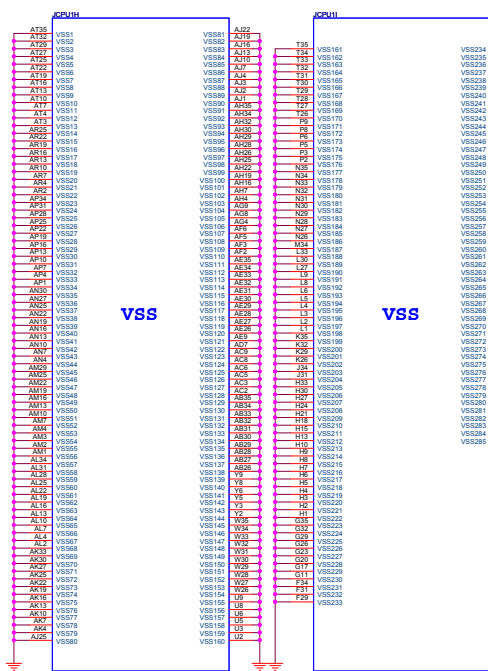
DDR_B_P84 (16) **DDR_B_P85** (16) **DDR_B_P86** (16) **DDR_B_P87** (16)

DDR_A_P88 (16) **DDR_A_P89** (16) **DDR_A_P90** (16) **DDR_A_P91** (16)

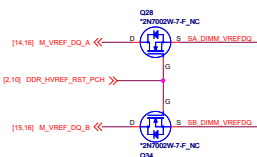
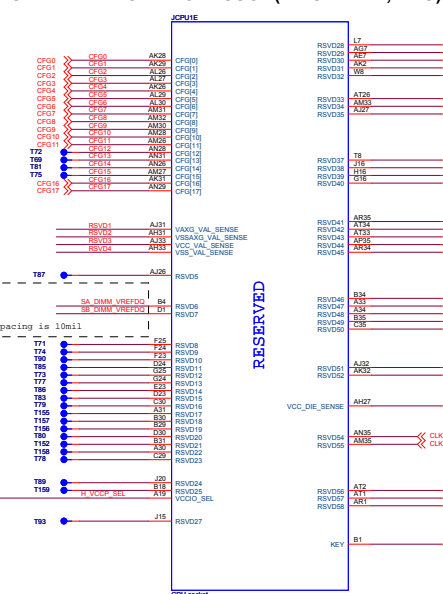
DDR_B_P88



SANDY BRIDGE PROCESSOR (GND)



SANDY BRIDGE PROCESSOR(RESERVED, CFG)

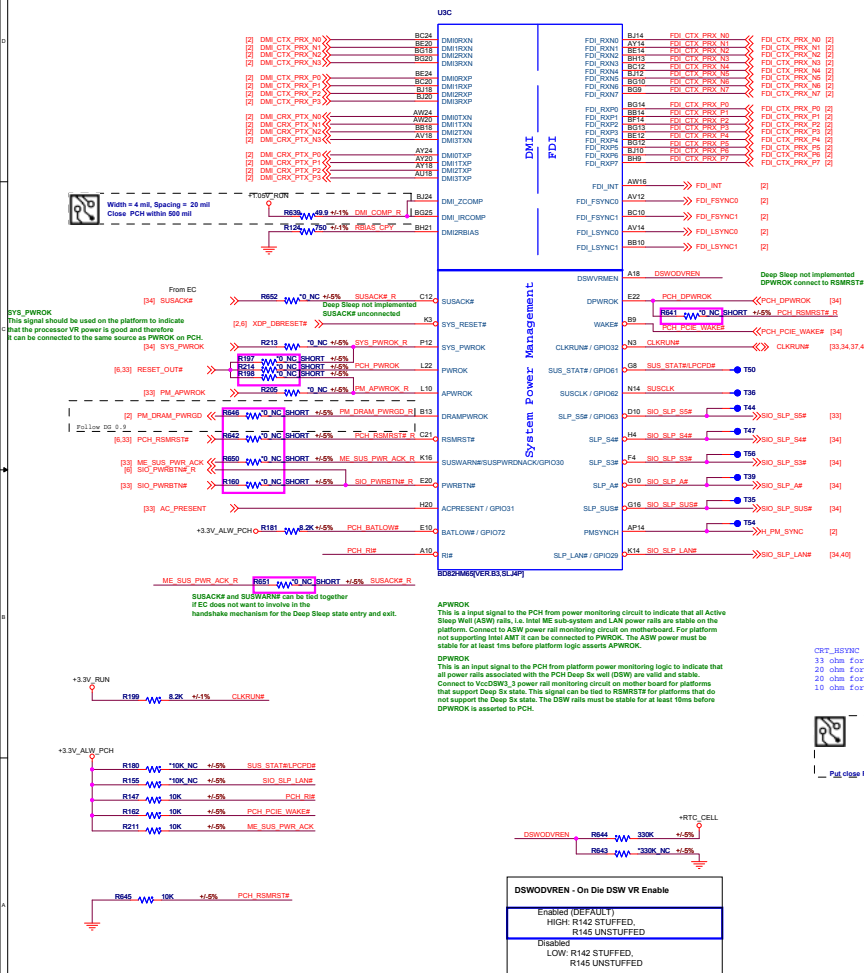


	1	0
CFG2 (PEG Static Lane Reversal)	Lan# definition matches socket pin map definition (Default Value)	Lan Reversed
CFG4 (Display Port Presence strap)	Disabled; No Physical Display Port attached to Embedded Display Port (Default Value)	Enabled; An external Display port device is connected to the Embedded Display port
CFG7 (PEG Deferr Training)	PEG Train immediately following xRRETSB of assertion (Default Value)	PEG Wait for BIOS for training

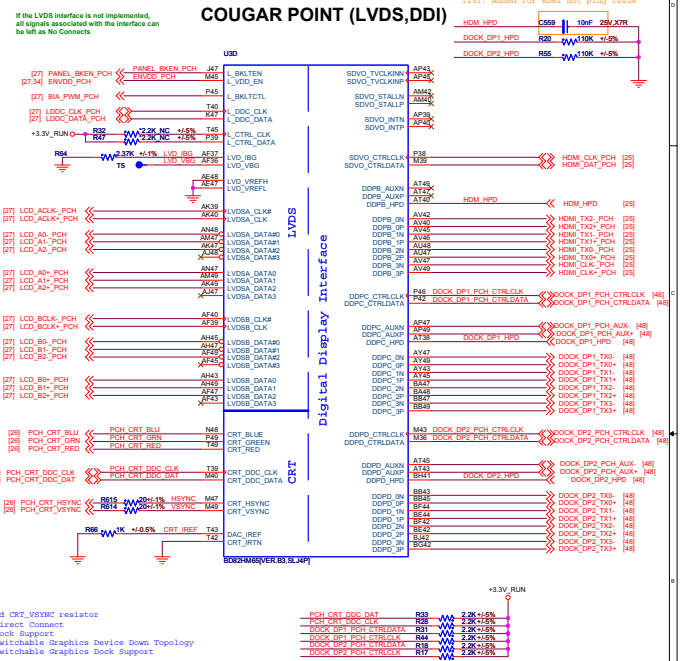
CFG[6:5] (PCIe Port Bifurcation Straps)	11	x16 - Device 1 functions 1 and 2 disable (Default Value)
	10	x8, x8 - Device 1 function 1 enable; function 2 disable
	01	Reserved - (Device 1 function 1 disable; function 2 enable)
	00	x8, x8, x4 - Device 1 function 1 and 2 enable



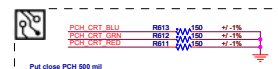
COUGAR POINT (DMI,FDI,GPIO)



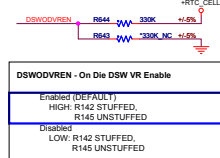
COUGAR POINT (LVDS,DDI)

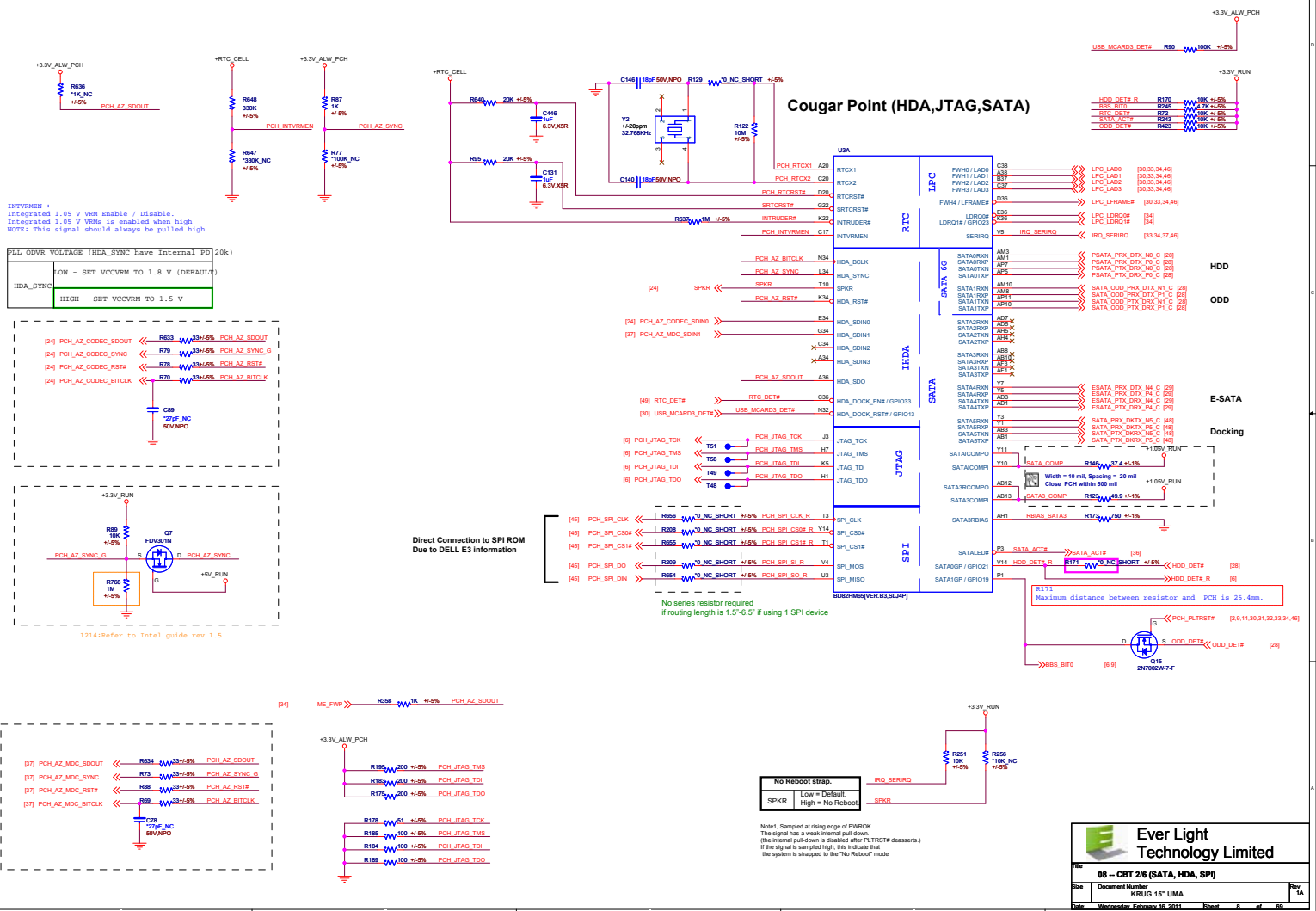


```
CRT_HSYNC and CRT_VSYNC resistor
33 ohm for Direct Connect
20 ohm for Dock Support
20 ohm for Switchable Graphics Device Down Topology
10 ohm for Switchable Graphics Dock Support
```

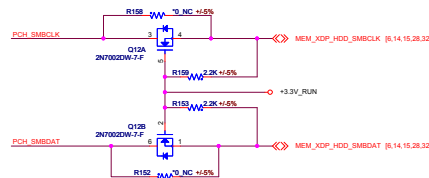
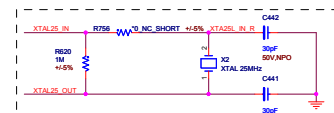
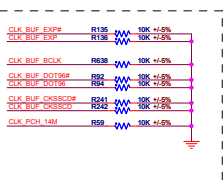


Put close PCH 500 mil

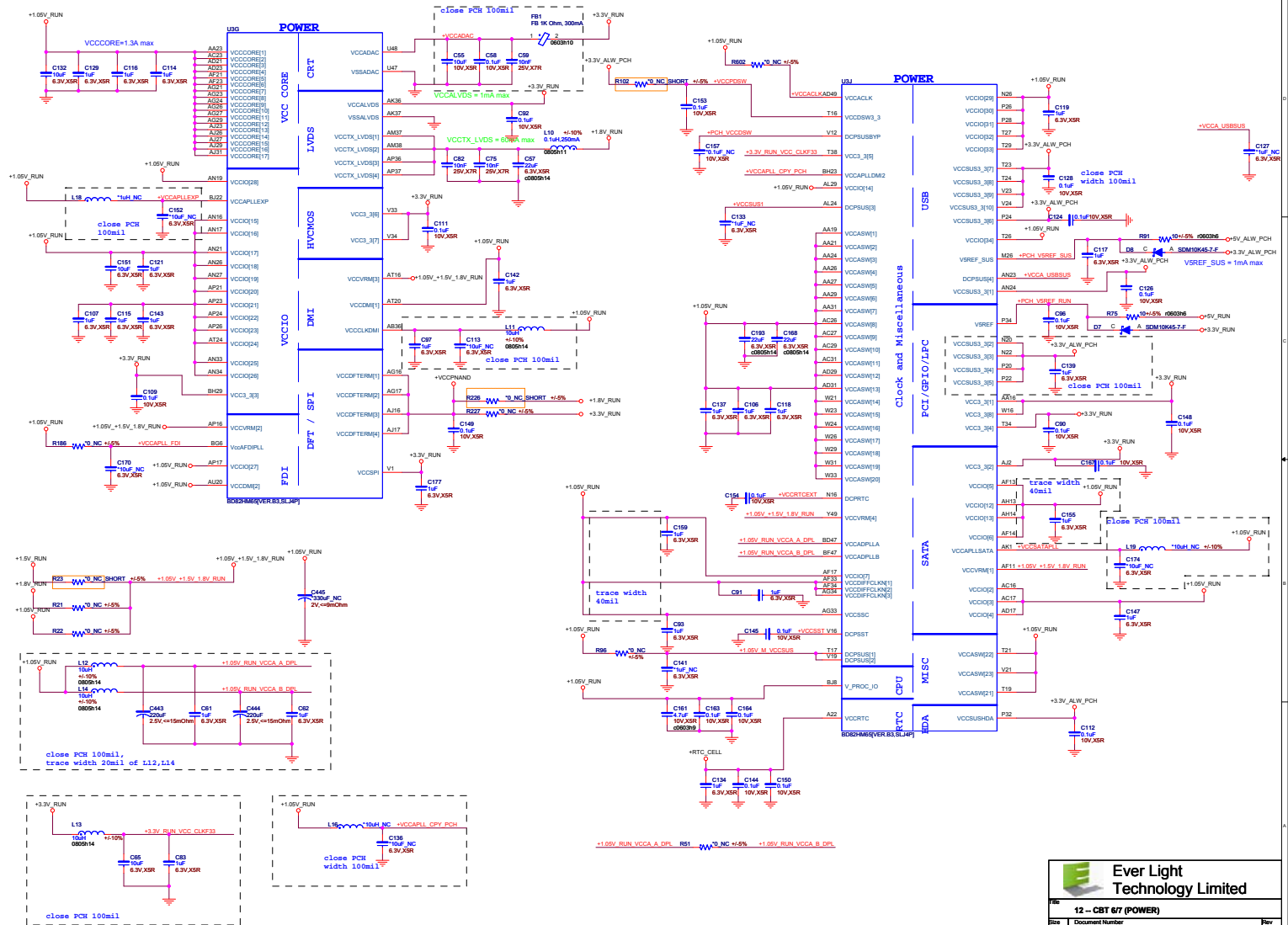




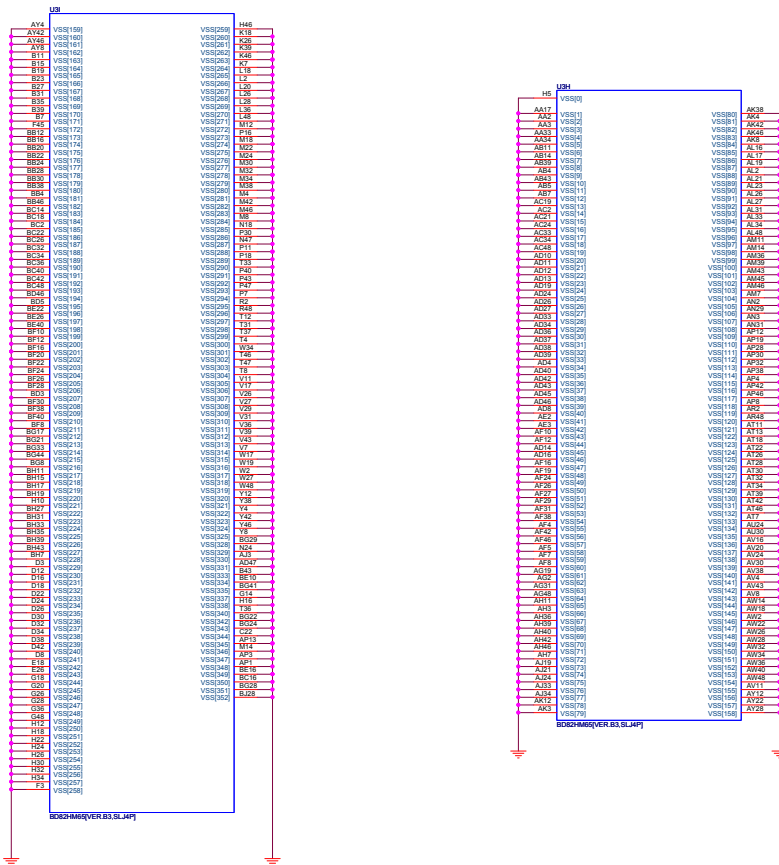
1128



1227: Pop R196 for Intel ME setting.

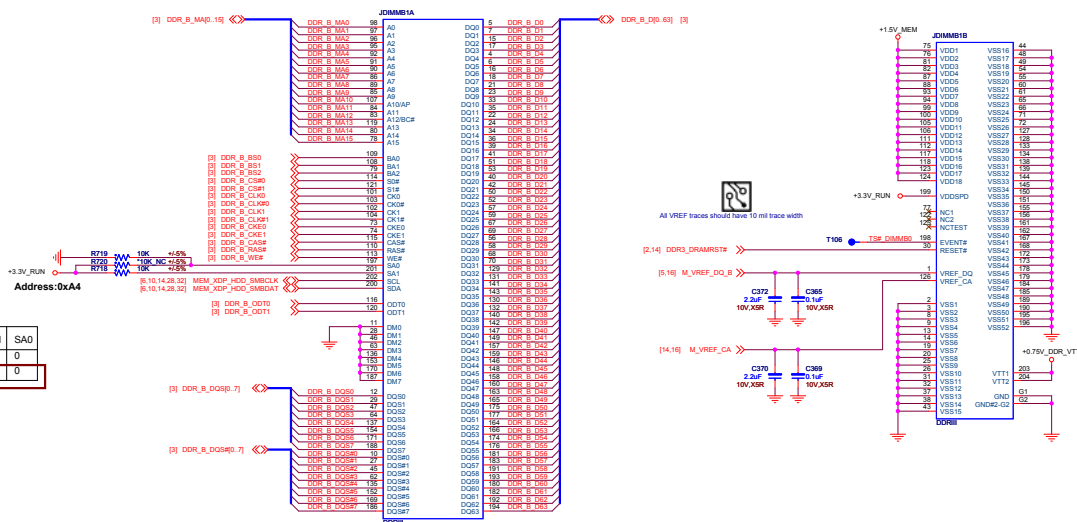
COGAR POINT (POWER)

Cougar Point (GND)

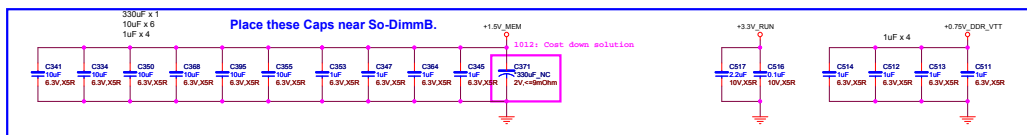


DDR3 Length Matching Formulas

Signal Group	Min Length	Max Length
Control-to-Clock	Clock - 0.5"	Clock - 0.0"
Command-to-Clock	Clock - 0.5"	Clock - 0.5"
Strobe-to-Clock	Clock - 0.5"	Clock - 1.0"
Data-to-Strobe (per byte lane)	Strobe - 20 mils	Strobe + 20 mils



+1.5V_SUS decoupling caps be located at the VDD pins of each SO-DIMM connector in the vicinity of the CMO. Clock and Control signals. Those capacitors should be placed on the same side of the motherboard as the SO-DIMM connector.

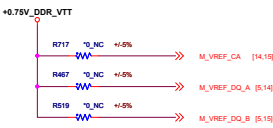


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File	15 - SODIMM-204P_JDIMMB	Rev	1A
Doc	Document Number		
Date	Wednesday, February 16, 2011	Sheet	15 of 59

M1: Fixed SO-DIMM VREF_DQ (Default)

M2: Programmable SODIMM VREFDQ




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 Ever Light Technology Limited		
File 17 - Blank Page (GPU)		
Size	Document Number XRUG 15" UMA	Rev 1A
Date: Wednesday, February 16, 2011 Sheet 17 of 59		

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		Ever Light Technology Limited	
File: 20 - Blank Page (GPU)			
Size	Document Number		Rev
	KRUG 15" UMA		1A
Date: Wednesday, February 16, 2011		Sheet	20 of 89

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		Ever Light Technology Limited	
File: 22 - Blank Page (GPU)			
Size	Document Number	Rev	
	KRUG 15" UMA	1A	
Date: Wednesday, February 16, 2011		Sheet	22 of 89

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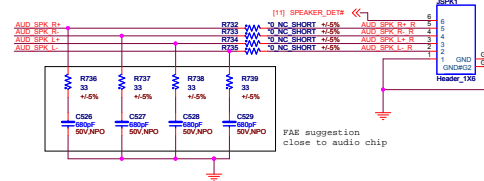
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File: 23 - Blank Page (GPU)			
Size	Document Number	Rev	
	KRUG 15" UMA	1A	
Date: Wednesday, February 16, 2011		Sheet	23 of 89



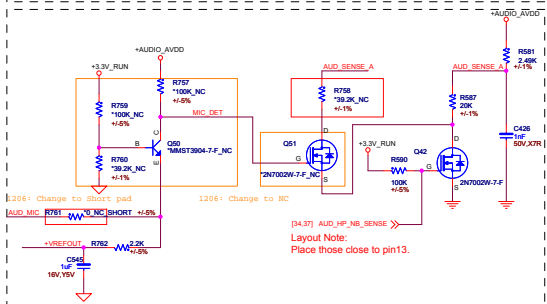
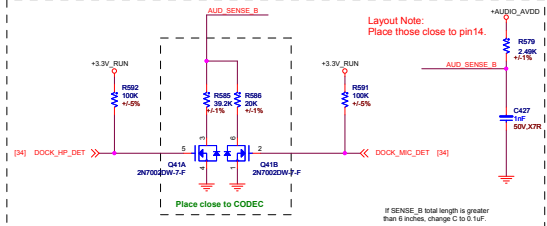
Layout Note:
Place caps close to codec.

Layout Note:
Place caps close to codec.

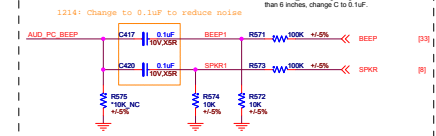
Speaker Connector



Keep those trace as widely as possible
that will help to decrease the Power Loss



PC BEEP



Ever Light
Technology Limited

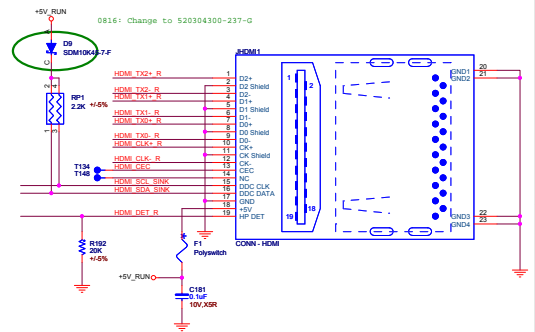
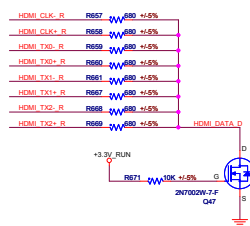
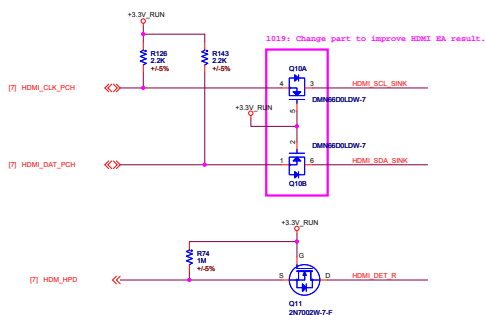
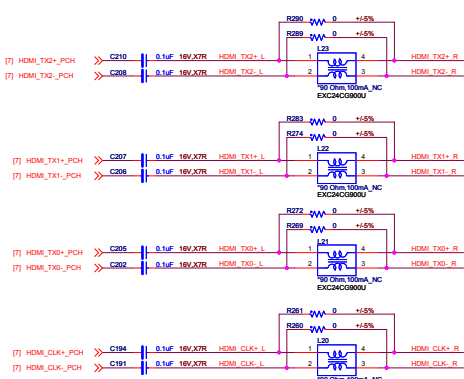
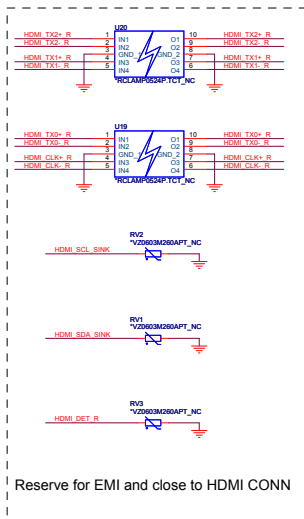
File	24 - S2HD908	Rev	1A
Size	Document Number	Thunder	
Date	Wednesday, February 16, 2011	Sheet	24 of 59

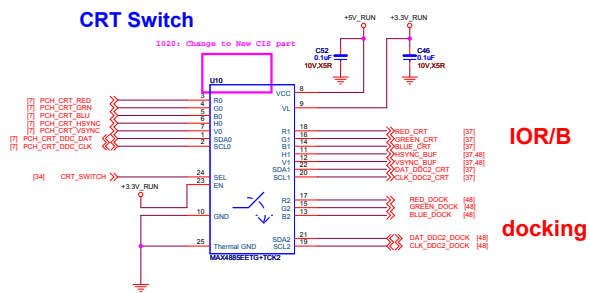
Colay Note
Default:uninstall R763,R758
Install R578
Second:uninstall R578
Install R763,R758

For EMI Request



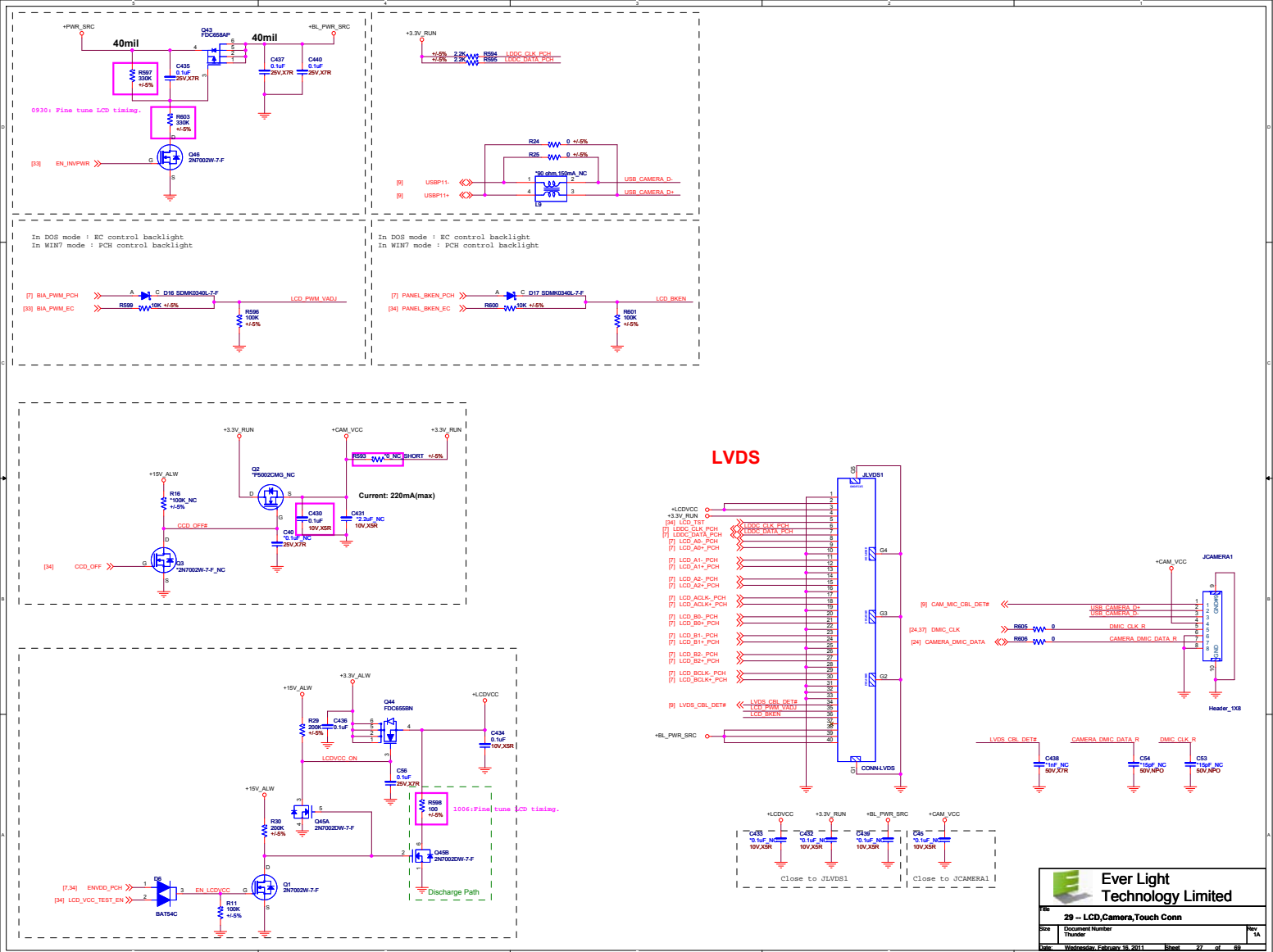
HDMI CONN



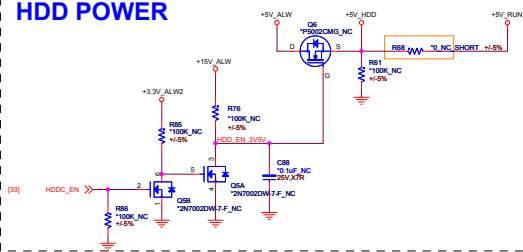


CRT Switch table

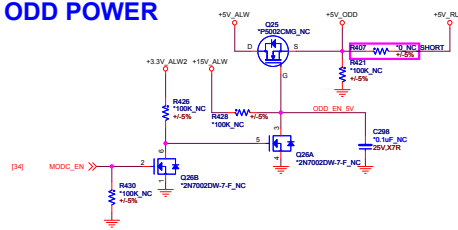
SEL	VGA signals	Switch
L	RGB[0] = RGB[1] SDA[0] = SDA[1] SCL[0] = SCL[1]	IOR/B
H	RGB[0] = RGB[2] SDA[0] = SDA[2] SCL[0] = SCL[2]	DOCK



HDD POWER

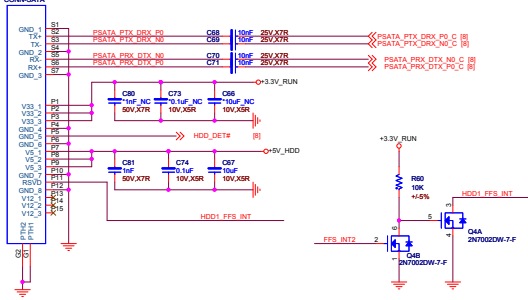


ODD POWER

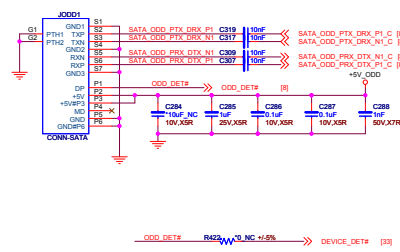


HDD Connector

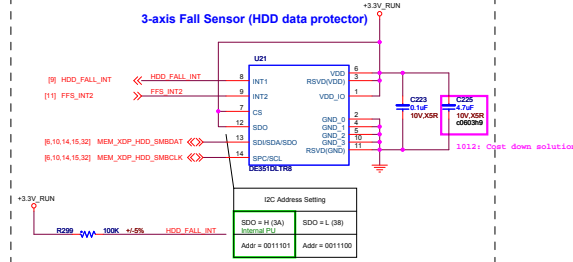
Main HDD



ODD Connector

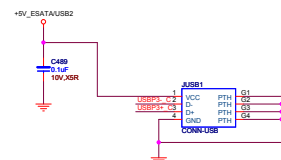


3-axis Fall Sensor (HDD data protector)

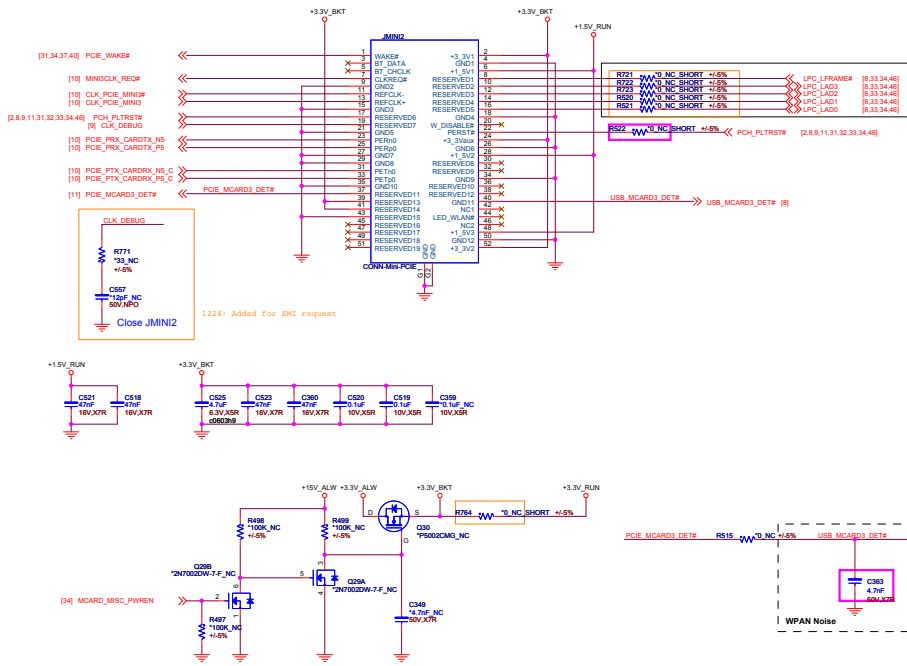


[34] ESATA_USB_PWR_EN#

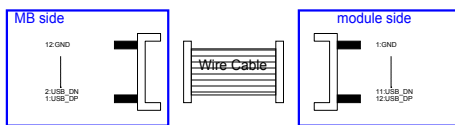
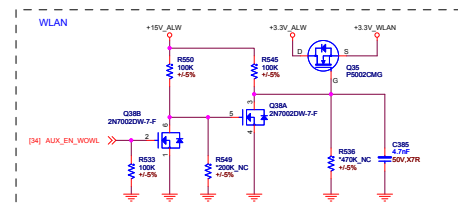
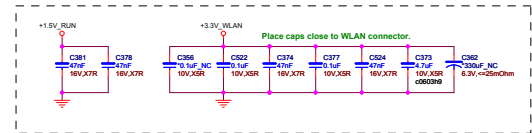
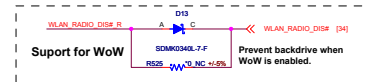
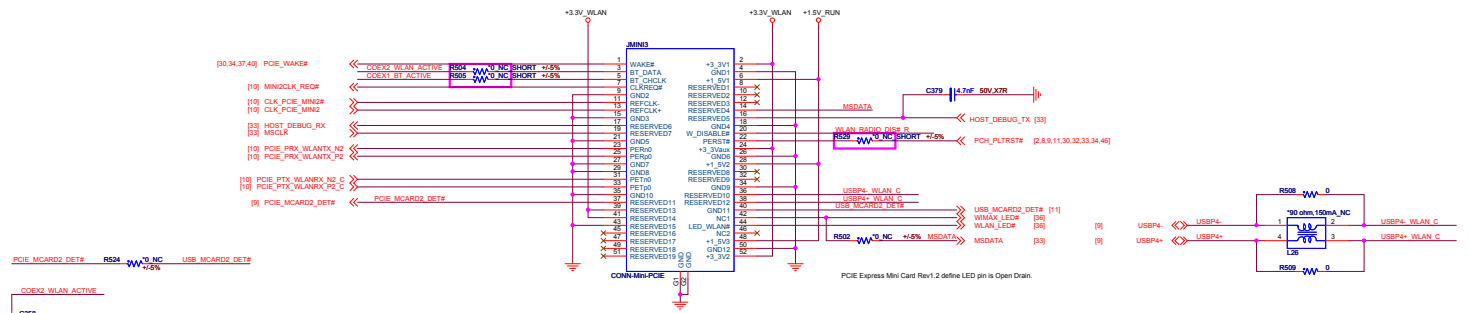
1006:Change U37 to GS46B4P10Z.



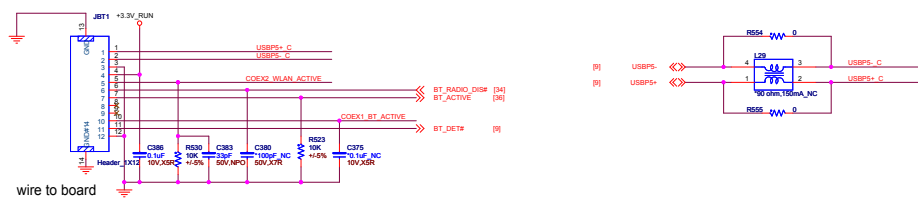
3rd MiniCard connector (Flash, half size) MiniCard connector



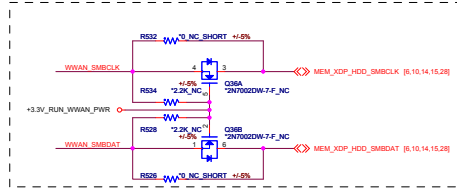
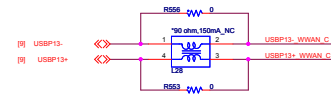
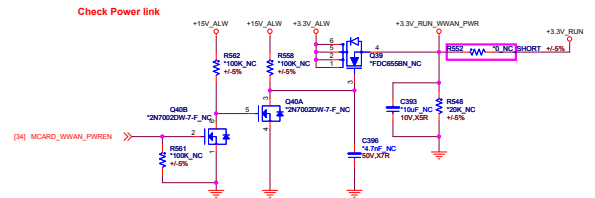
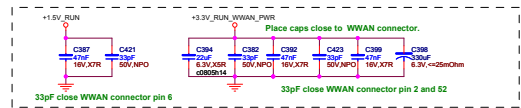
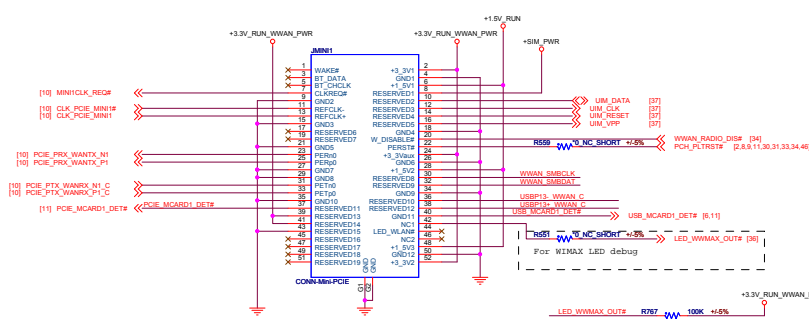
2nd MiniCard connector (WLAN, half size)
MiniCard WLAN connector

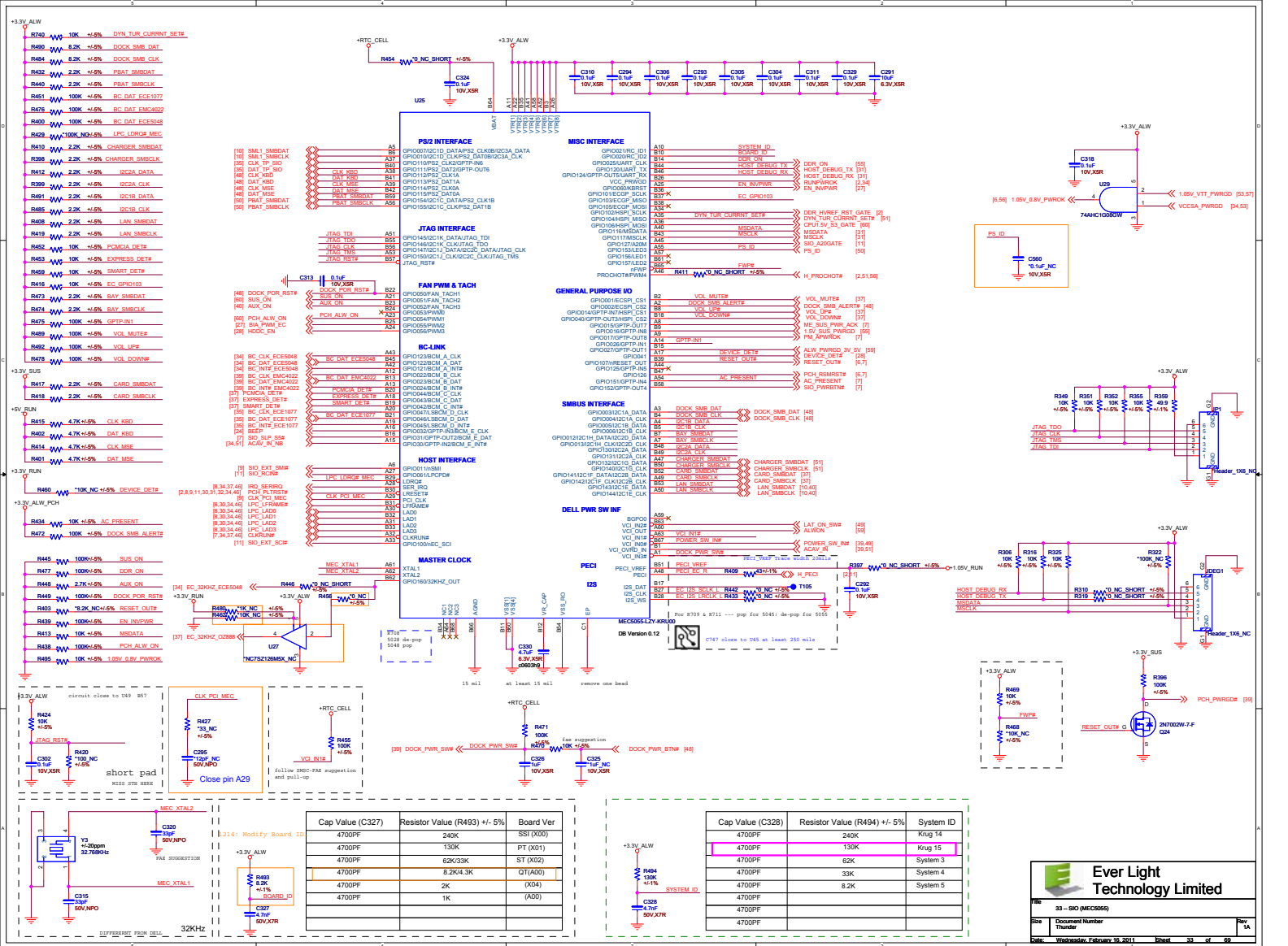


Bluetooth Support Blarney stone 375

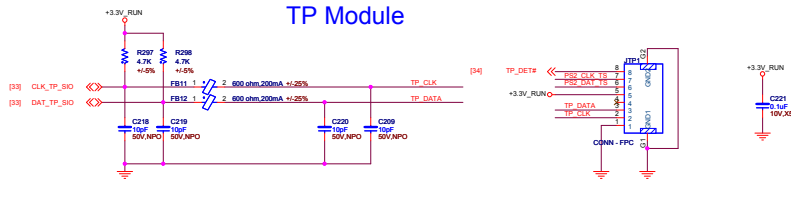


MiniCard WWAN connector

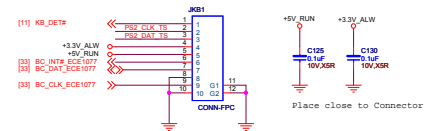


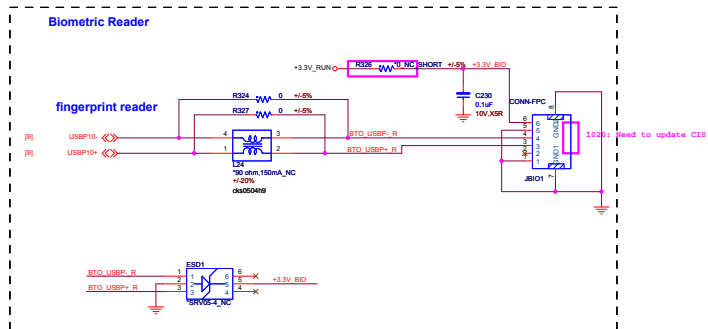


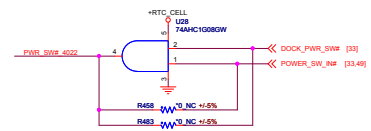
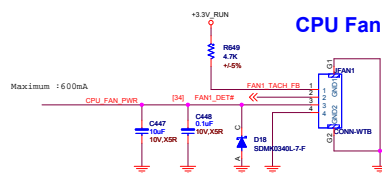
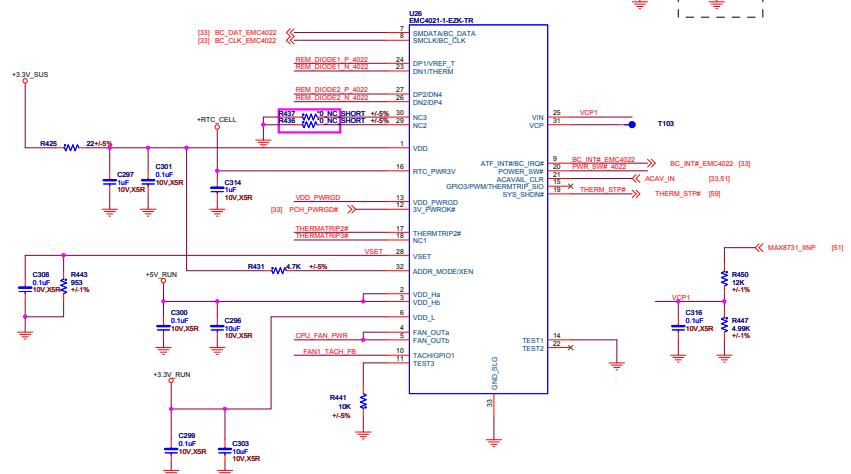
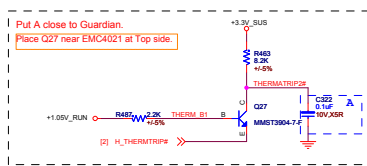
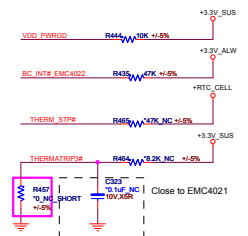
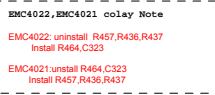
TP Module

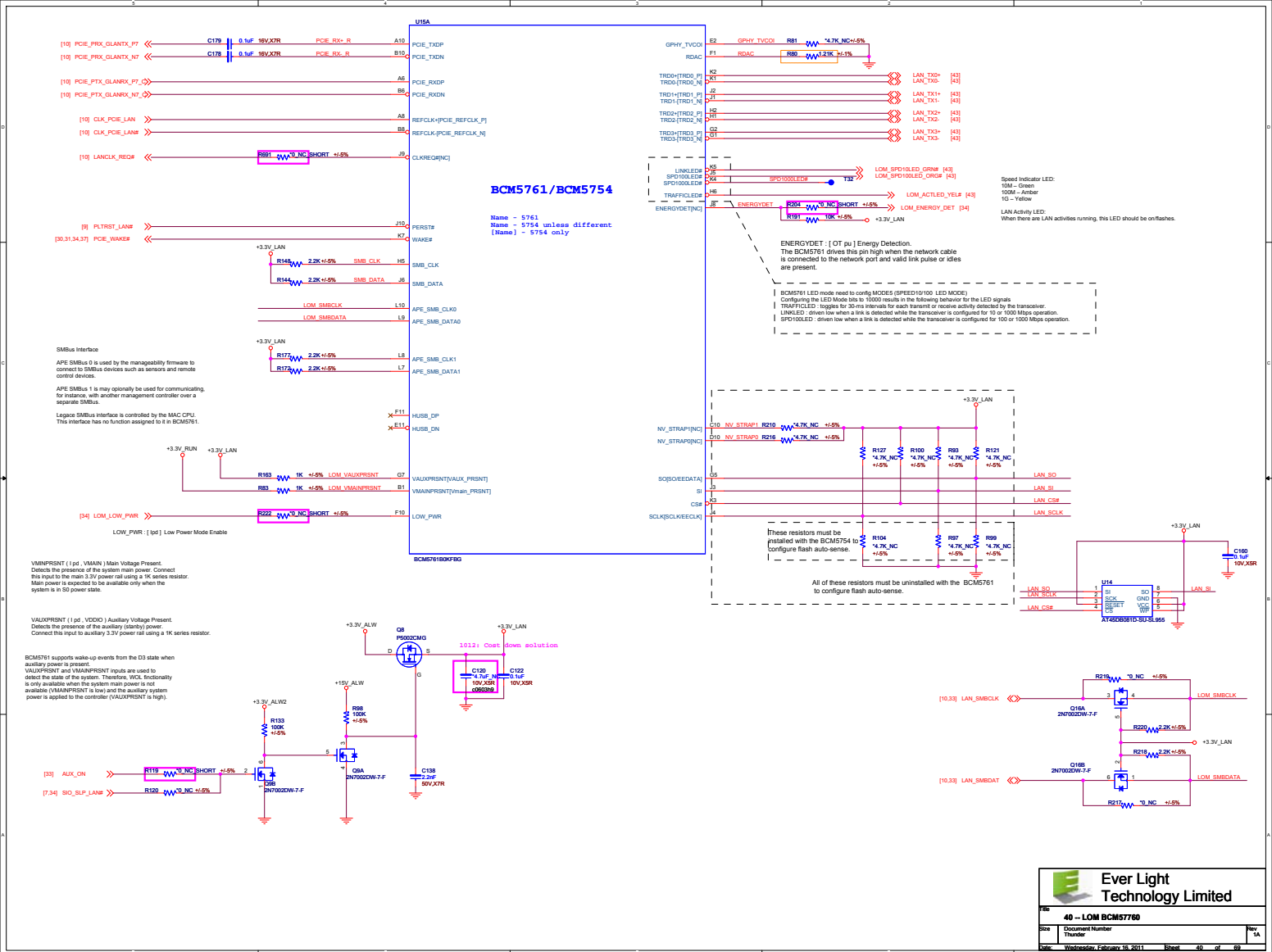


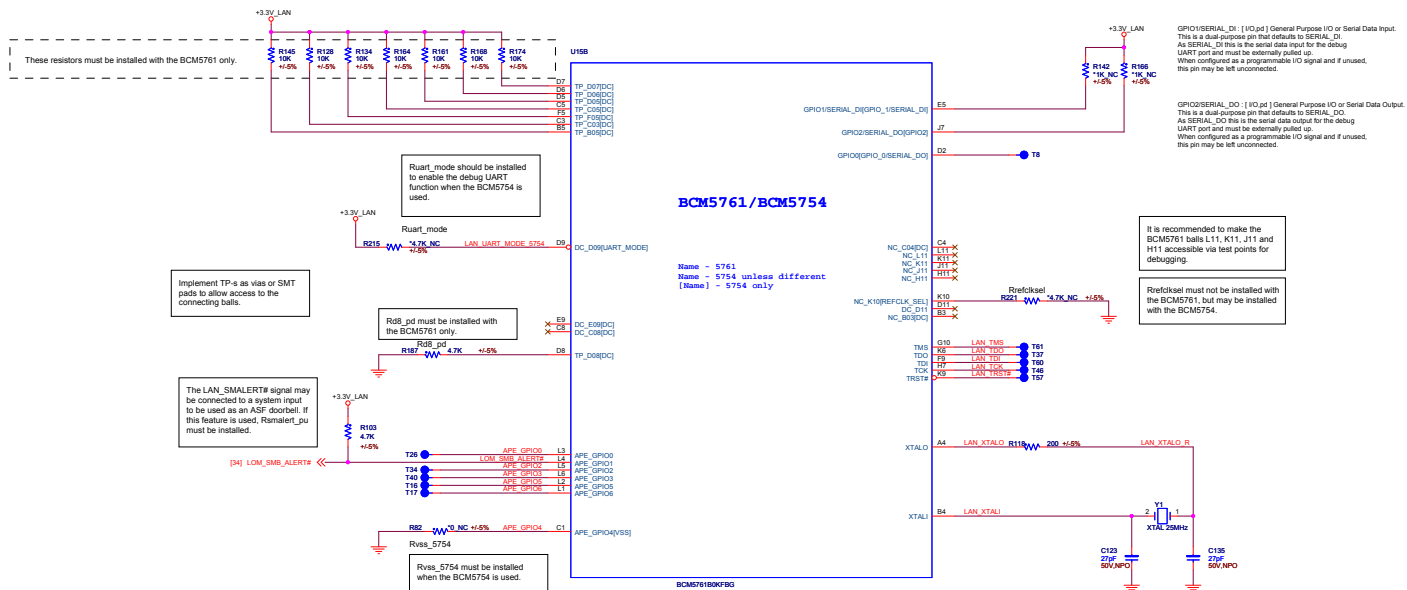
Keyboard Module

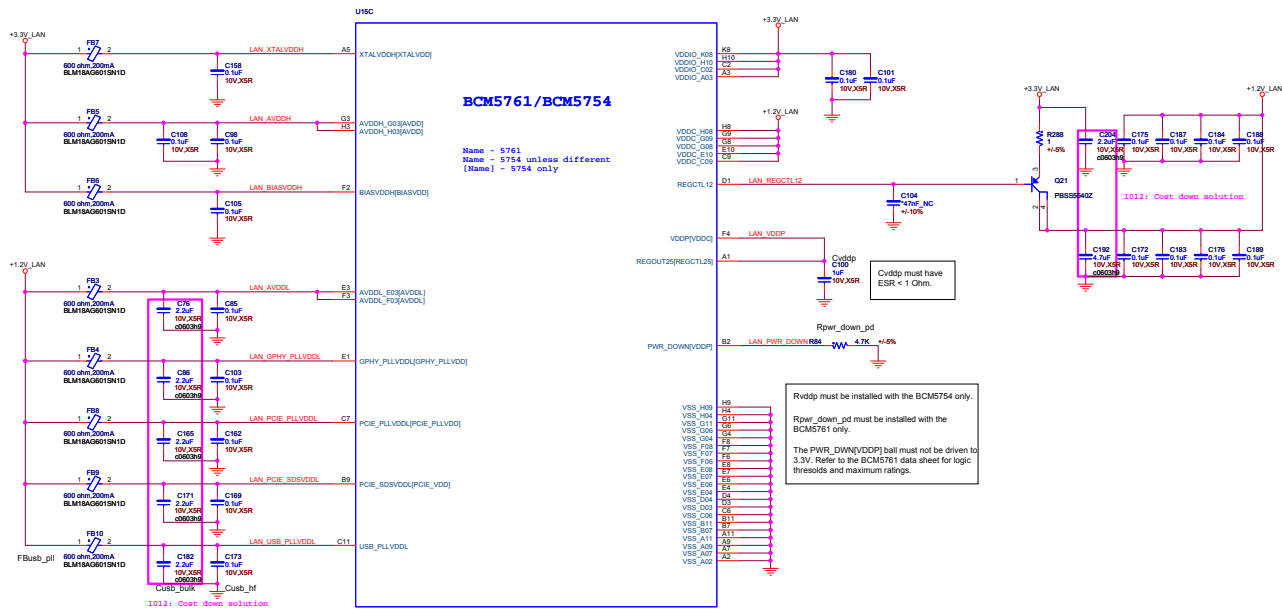








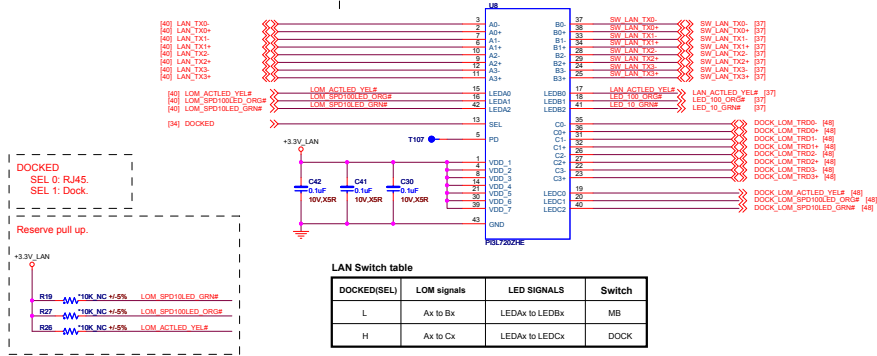




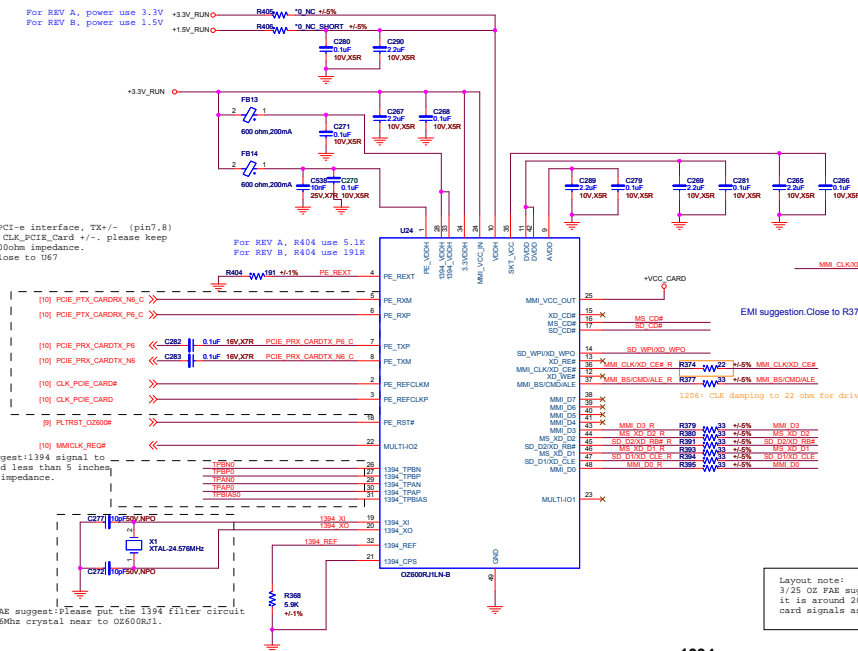
If the BCM5761 is installed, Fusb_pll, Cusb_bulk and Cusb_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, Fusb_pll, Cusb_bulk and Cusb_hf may be uninstalled.

SnRt is a suggested value.
Actual value will be system dependent.
Must use 0603 package for lower DC resistance.

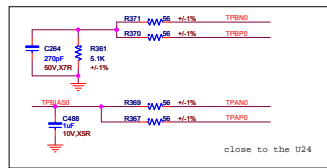


For REV A, power use 3.3V
For REV B, power use 1.5V



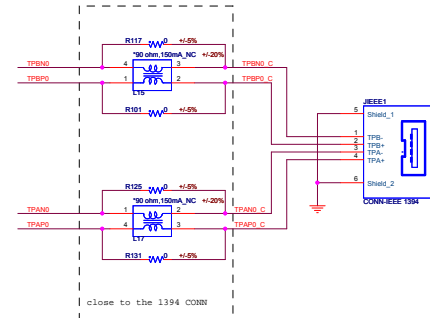
Card Reader Conn Pin definition

NO	FOR	Pin Assign	Function
01	SD	#9	SD-DAT2
02	MemoryStick	#10	MS-VSS
03	SD/MMC	#1	SD-CD/DAT3 MMC-RSV
04	MemoryStick	#9	MS-VCC
05	MemoryStick	#8	MS-SCLK
06	SD/MMC	#2	SD-CHD MMC-CMD
07	MemoryStick	#7	MS-DATA3
08	MemoryStick	#6	MS-INS
09	SD/MMC	#3	SD-VSS MMC-VSS1
10	MemoryStick	#5	MS-DATA2
11	SD/MMC	#4	SD-VDD MMC-VDD
12	MemoryStick	#4	MS-DATA0
13	MemoryStick	#3	MS-DATA1
14	SD/MMC	#5	SD-CLK MMC-CLK
15	MemoryStick	#2	MS-BS
16	MemoryStick	#1	MS-VSS
17	SD/MMC	#6	SD-VSS MMC-VSS2
18	SD/MMC	#7	SD-DAT0 MMC-DAT
19	SD	#8	SD-DAT1
20	SD	CD	SD-CD
21	SD	GND	SD-GND
22	SD	SW_WP	SD-WP(SW)

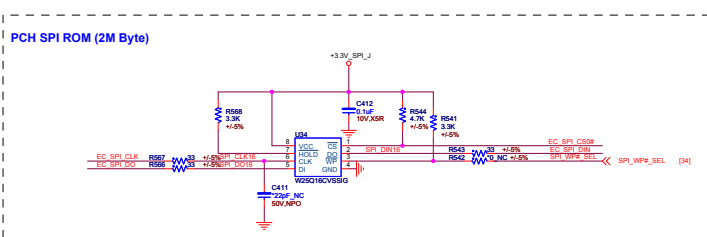
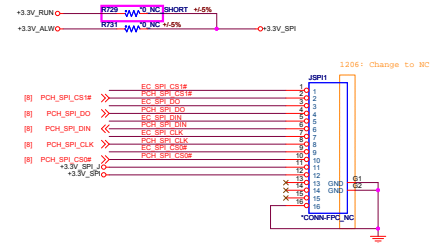


1394a

Layout note:
3/25 OZ FAE suggest:Please care the SD interface layout, it is around 208MHz clock speed, please control the SD card signals as equal length.



PCH, EC SPI ROM For BIOS (4M Byte)

[illegible]

Pin	Signal
1	PCH_SPI_CS1#
2	PCH_SPI_CS1#
3	PCH_SPI_DO
4	PCH_SPI_DO
5	PCH_SPI_DIN
6	PCH_SPI_DIN
7	PCH_SPI_CLK
8	PCH_SPI_CLK
9	PCH_SPI_CS0#
10	PCH_SPI_CS0#
11	+3.3V_SPI
12	+3.3V_SPI
13	GND
14	GND
15	GND
16	GND

CONN-FPC

1206: Change to short pad.

EC SPI CS# R724 0 NC SHORT +5% PCH SPI CS#

EC SPI DO R725 0 NC SHORT +5% PCH SPI DO

EC SPI DIN R727 0 NC SHORT +5% PCH SPI DIN

EC SPI CLK R728 0 NC SHORT +5% PCH SPI CLK

EC SPI CS# R729 0 NC SHORT +5% PCH SPI CS#

+3.3V_SPL R730 0 NC SHORT +5% PCH SPI

Put close to JSPI1

1206: Change to short pad.

EC SPI CS# R724 0 NC SHORT +5% PCH SPI CS#

EC SPI DO R725 0 NC SHORT +5% PCH SPI DO

EC SPI DIN R727 0 NC SHORT +5% PCH SPI DIN

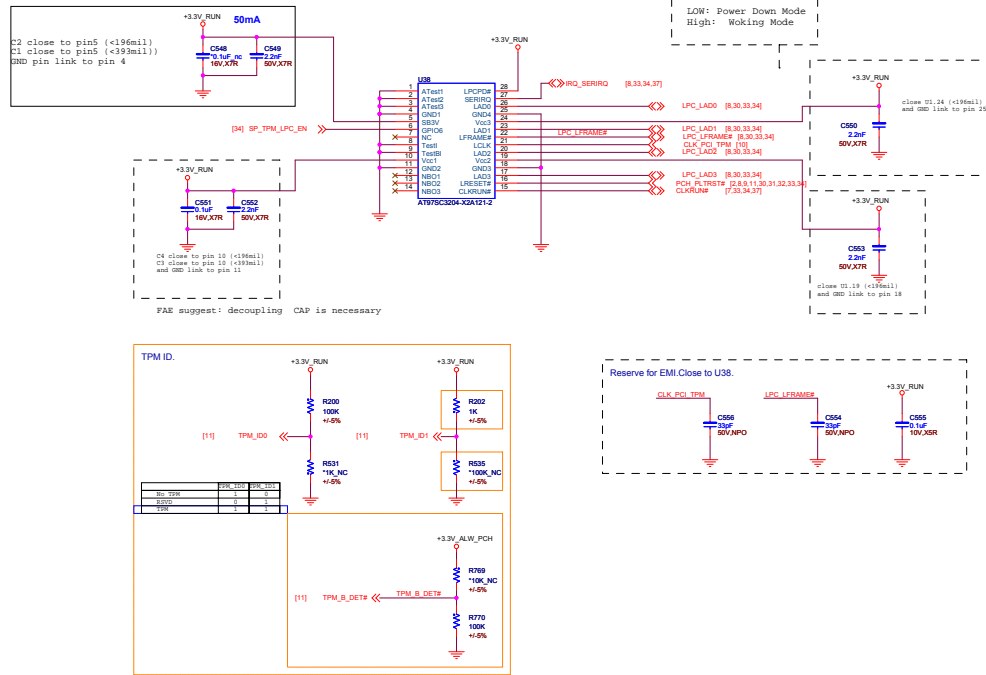
EC SPI CLK R728 0 NC SHORT +5% PCH SPI CLK

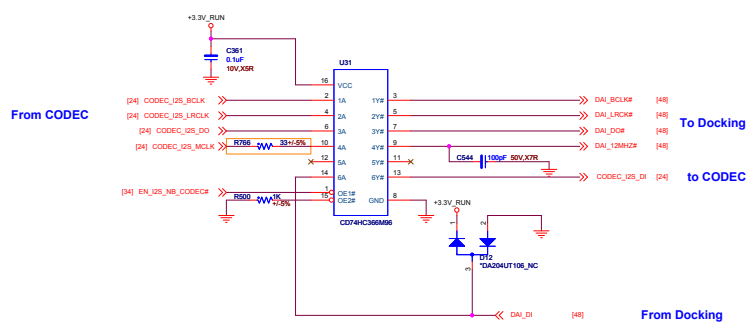
EC SPI CS# R729 0 NC SHORT +5% PCH SPI CS#

+3.3V_SPL R730 0 NC SHORT +5% PCH SPI

Put close to JSPI1

China TPM : ATMEL (TEMP SYMBOL)

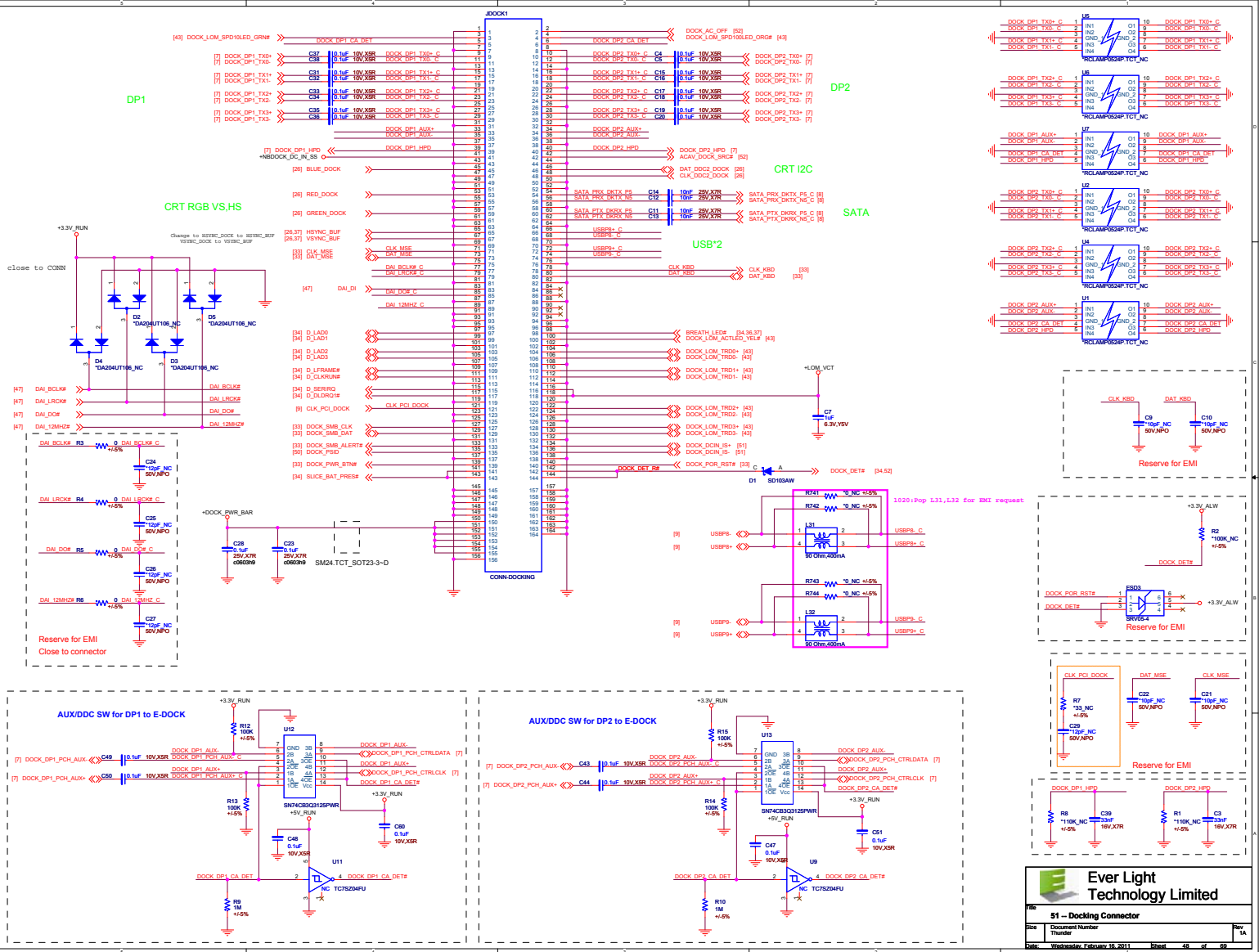


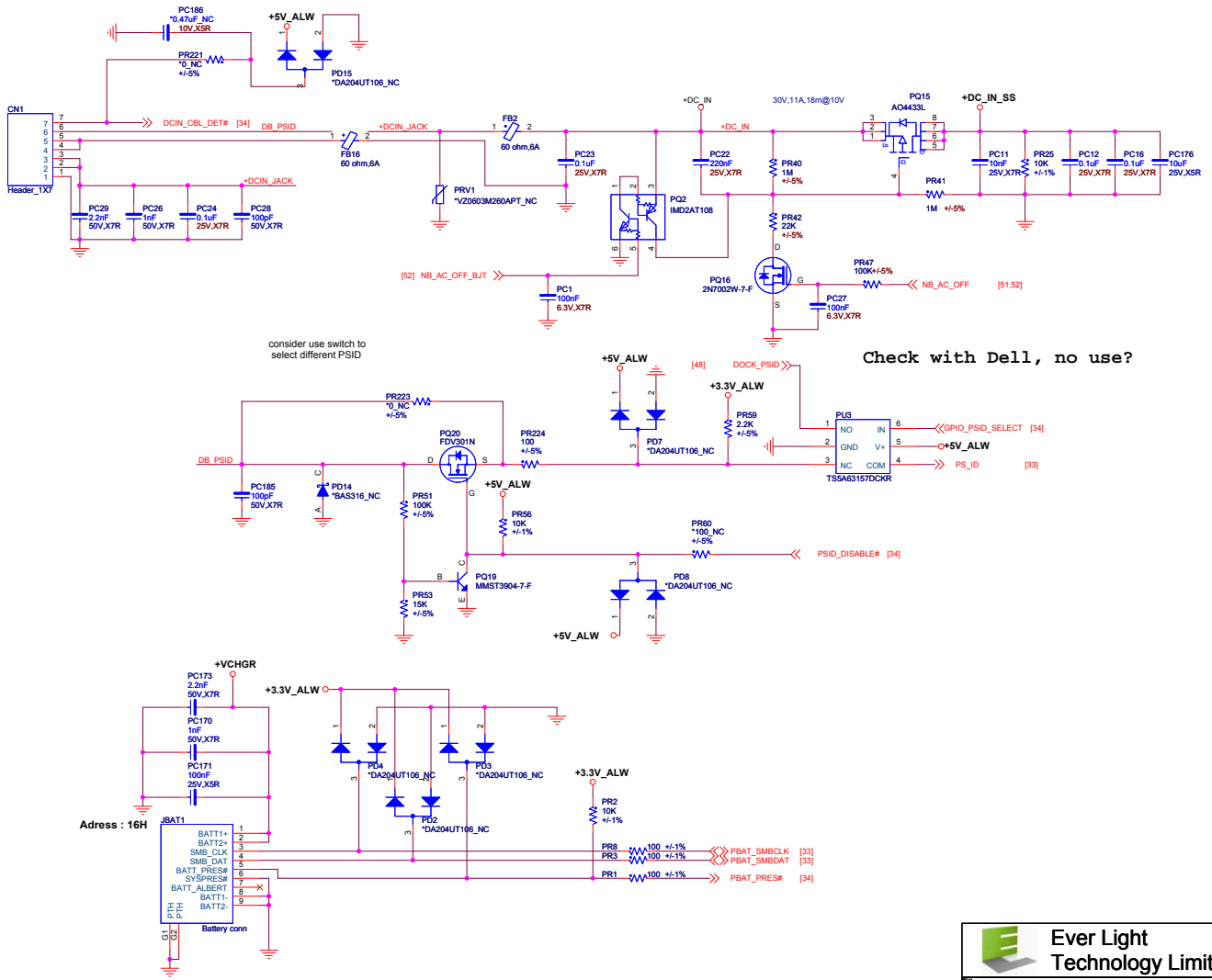


CD74HC366M96 table

INPUTS			OUTPUTS(Y)
OE1#	OE2#	A	HC366
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

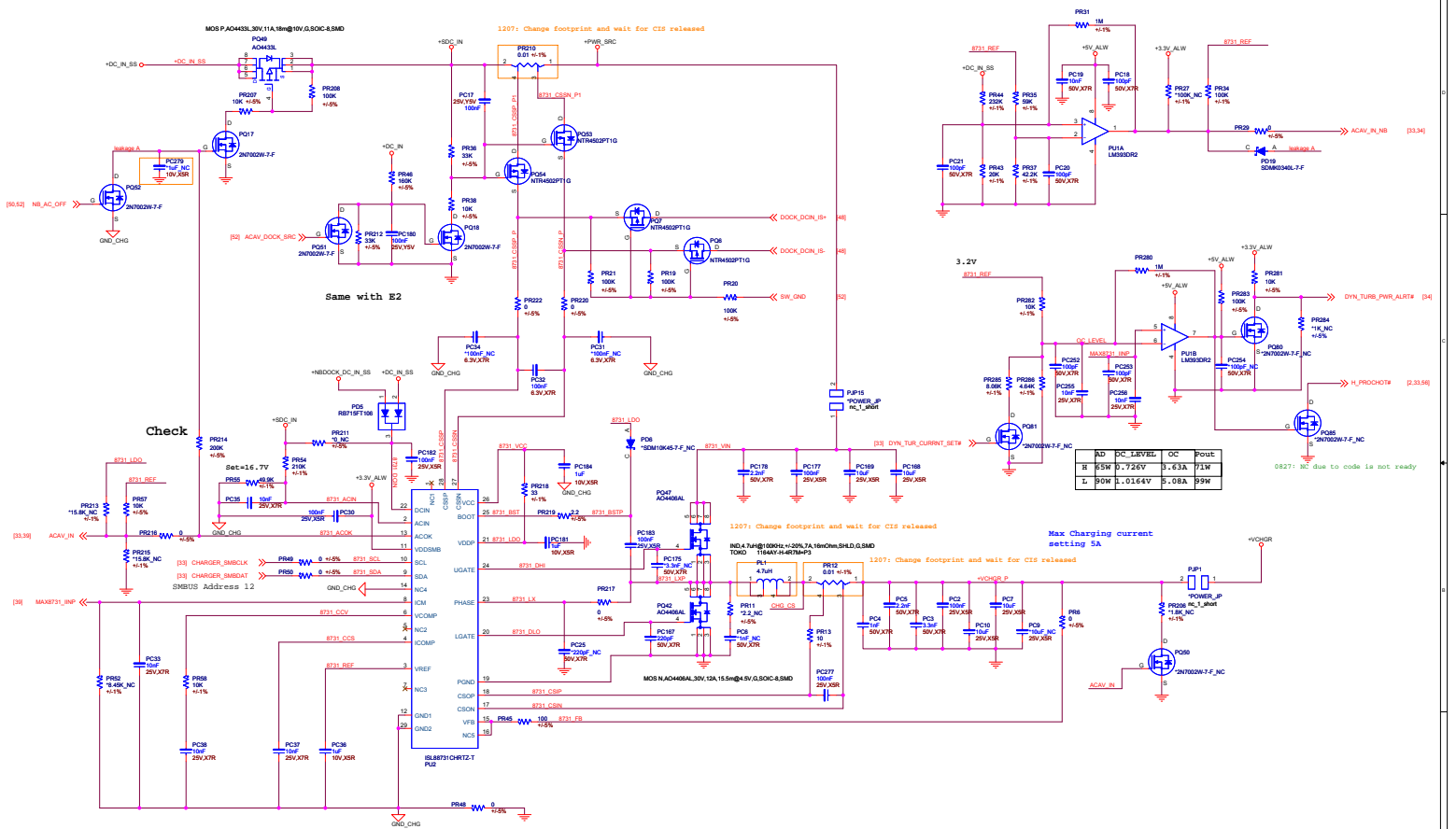
NOTE:
Z=High impedance (OFF) state





consider use switch to select different PSID

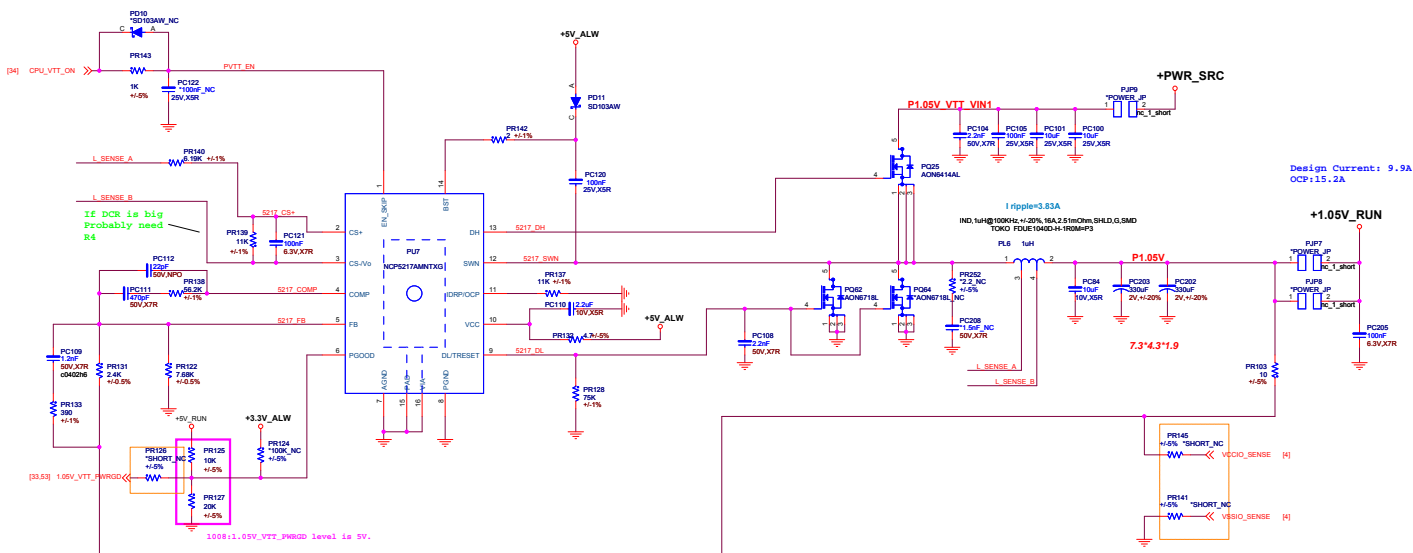
Check with Dell, no use?





Design Current: 23.1A
OCP: 35.5A
+VCC_GFXCORE





D

D

C

C

B

1

A

A



Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	321-328
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-130
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-574
5. The Effect of Catalyst on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-685

58 -- PW_Blank for Ext.GPU

Size

Document Number
KRUG 15" UMA

Rev

Rev
1A

Date: Wednesday, February 16, 2011 Sheet 58 of 69

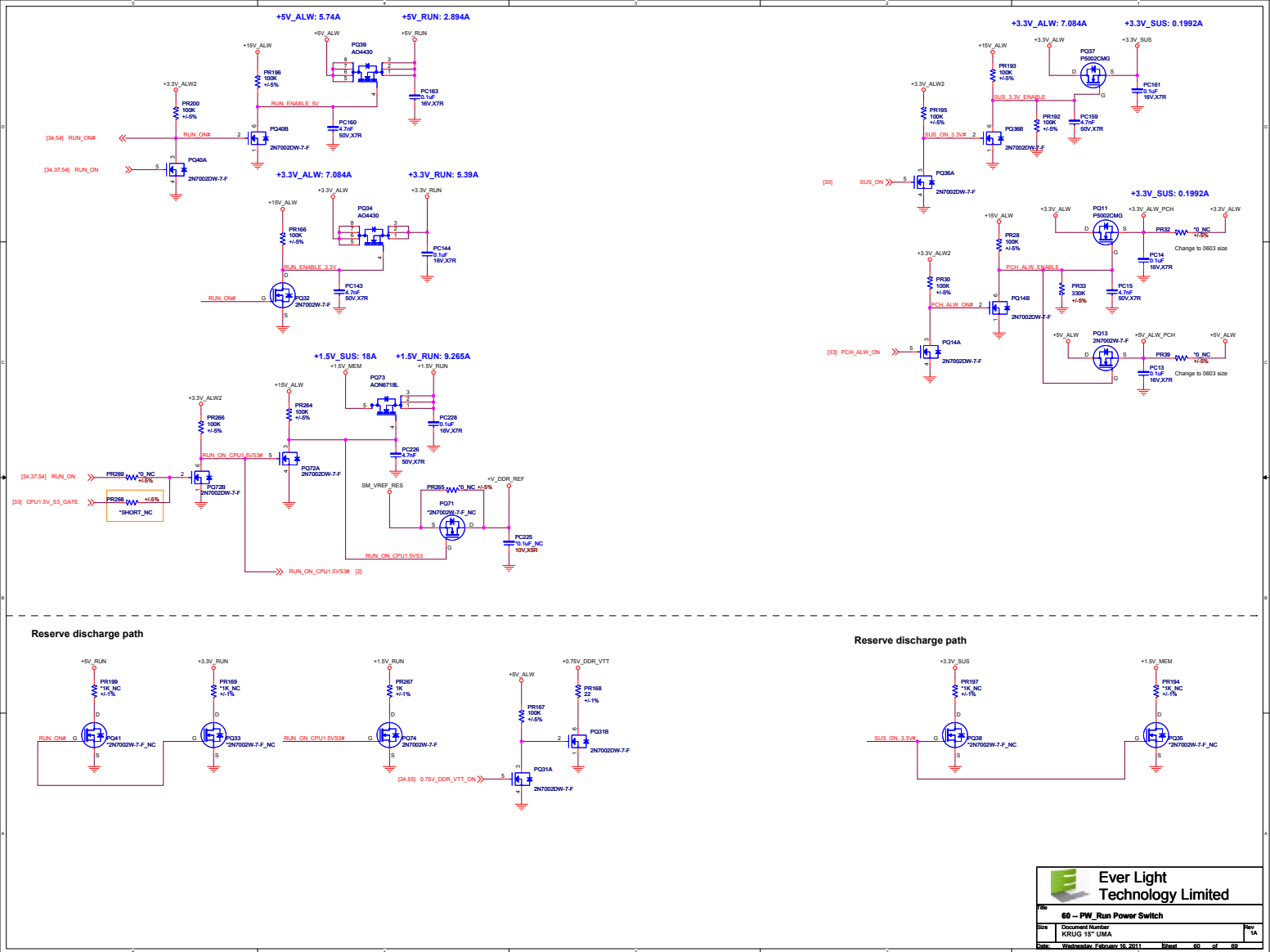
5

4

3

2

1



D

D

C

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Ever Light
Technology Limited

Title

61 -- PW_Blank

Size

Document Number
KRUG 15" UMA

Rev
1A

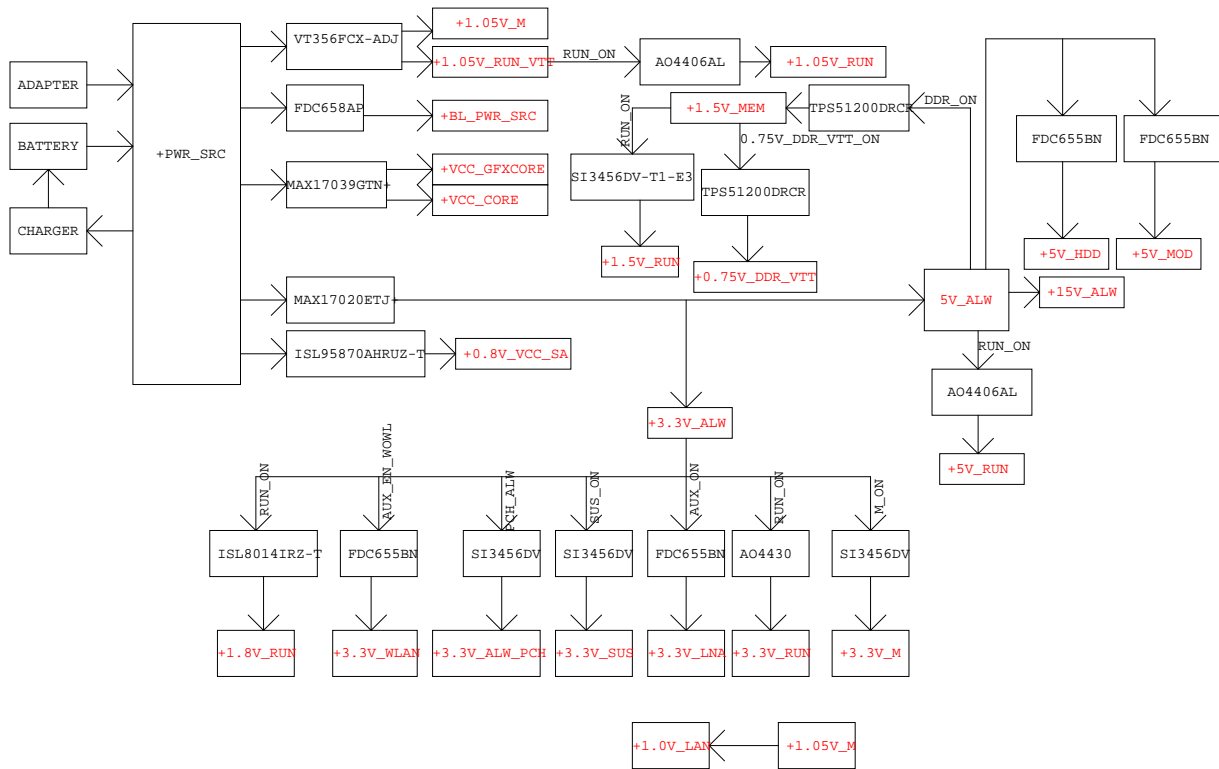
Date: Wednesday, February 16, 2011 Sheet 61 of 69

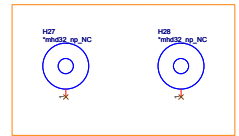
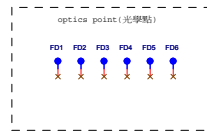
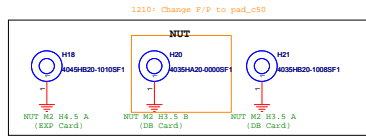
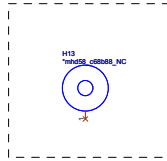
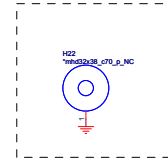
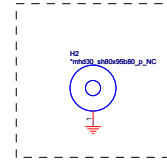
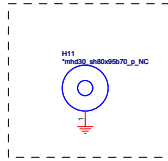
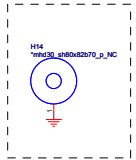
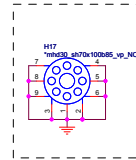
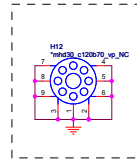
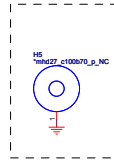
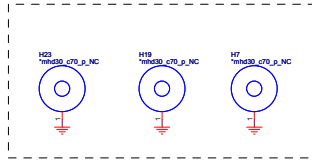
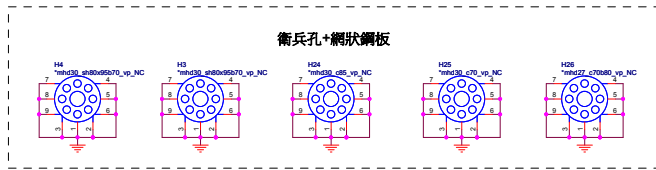
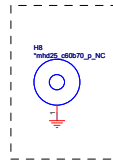
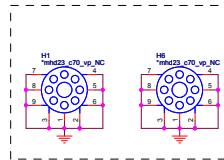
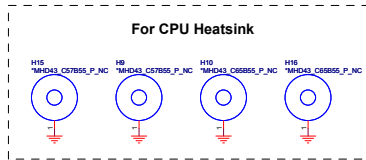


Title	62 - PW_Blank
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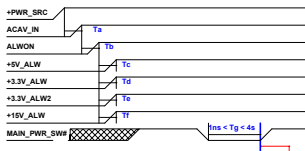
Size	Document Number KRUG 15" UMA
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Date: Wednesday, February 16, 2011 Sheet 62 of 69

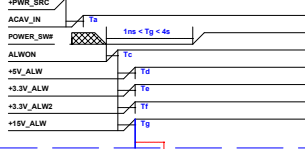




[AC in]



[Battery only, AC absent]



EC pay attention timing

UMA Power On Sequence

[AC in]

ITEM	Measure Point	Time
T1	+PWR_SRC	T1
T2	ACAV_IN	T2
T3	ALWON	T3
T4	+5V_ALW	T4
T5	+3.3V_ALW	T5
T6	+3.3V_ALW2	T6
T7	+15V_ALW	T7
T8	MAIN_PWR_SW#	N/A

[Battery only, AC absent]

ITEM	Measure Point	Time
T1	+PWR_SRC	T1
T2	ACAV_IN	T2
T3	ALWON	T3
T4	+5V_ALW	T4
T5	+3.3V_ALW	T5
T6	+3.3V_ALW2	T6
T7	+15V_ALW	T7
T8	MAIN_PWR_SW#	N/A

ITEM	Measure Point	Time
T1	MAIN_PWR_SW#	T1
T2	PCH_ALW_ON	T2
T3	+3.3V_ALW_PCH	T3
T4	+3.3V_ALW_PCH	T4
T5	PCH_RSMRST#	T5
T6	AC_PRESENT	T6
T7	SIO_PWRBTN#	T7
T8	SIO_SLP_S#	T8
T9	SIO_SLP_S#	T9
T10	SUS_ON	T10
T11	+3.3V_SUS	T11
T12	AUX_EN_WOVL	T12
T13	SIO_SLP_S#	T13
T14	DDR_ON	T14
T15	+1.5V_MEM	T15
T16	SIO_SLP_S#	T16
T17	SIO_SLP_S#	T17
T18	RUN_ON	T18
T19	RUN_ON	T19
T20	RUN_ON	T20
T21	RUN_ON	T21
T22	+1.5V_RUN	T22
T23	RUN_ON	T23
T24	CPU_VTT_ON	T24
T25	+1.05V_RUN	T25
T26	+1.05V_VTT_PWRGD	T26
T27	+0.85V_RUN	T27
T28	1.05V_0.8V_PWRGD	T28
T29	CPU1SV_S3_GATE	T29
T30	+1.5V_CPU_VDDQ	T30
T31	0.75V_DDR_VTT_ON	T31
T32	+0.75V_DDR_VTT	T32
T33	RUNPWRK	T33
T34	PM_APWRK	T34
T35	RESET_OUT#	T35
T36	PM_DRAM_PWRGD	T36
T37	H_CUPWRGD	T37
T38	MMVP_VR_ON	T38
T39	MMVP_VR_ON	T39
T40	+VCC_CORE	T40
T41	MMVP_PWRGD	T41
T42	SYS_PWRGD	T42
T43	SYS_PWRGD	T43

Change List						
Item	Date	T	Page#	Issue Description	Solution Description	Rev
				A00		
01		PWR		Delete Power Jump.	Change Power Jump to short pad.	A00
02			P39	Edit thermal diode note.		
03			P40	IEEE test fail.	Change R80 to 1.2K.	
04		EE	P45	SCN Changed	Change R744-R728,R730 to shortpad,de pop J8P11.	
05			P39	Change eSATA connector part number.	Change eSATA connector part number.	
06			P02	SCN Changed	De pop R273,R304,R314,R674-R678,R682,R684	
07			P06	SCN Changed	Remove XDP component,change R107-R112,R115,R116,R230-R236,R8230-R240 to NC	
08		EE	P06	SCN Changed	Change R284-R286,R302,R303,,R307,R311-R313,R105,R106,R113,R114,R237 to NC	
09			P24	SCN Changed	Change R761 to Short pad	
10			P24	SCN Changed	Change R757,R759,R760,Q50,Q51 to NC	
11			P44	Design Changed	CLK damping to 22 ohm (R374) for driving validation	
12			P51	Design Changed	Change P/N and PP for PR12,PR210,PL1 and wait for CIS released.	
13		PWR	P34	Design Changed	ADD R765 100K ohm for power request	
14			P49	Delete Power switch SW1.	Delete Power switch SW1.	
15			P11	TPM only	Pop R202 and De-pop R535	
16			P37	TPM only	Delete JTPM1,C541-C543,C376	
17			P46	Change TPM SCN to NB	Add U38,C548-C556 for TPM SCN changed.	
18		EE	P47	SCN Changed	Add R766 between U31 and Singal "ODDRC_I2S_MCLK"	
19			P64	Design Changed	Change H20 to new f/p mhd11_c50b_paste	
20			P46	TPM only	Move TPM ID table to Page46.	
21			P51	Power Changed	Reserve IuF(PC279) at Leakage A,let it will be low after +3.3V_ALW turn on.	
22			P36, P32	Wlan LED is lighting when WWAN module insert after AC-IN.	Add mosfet (Q52) and Res 100K (R767) to control LED .	
23			P37	Add 2 pin connector (CN18)	Add 2 pin connector (CN18)	
24			P36	LED Current & Brightness adjust	Change R588 & R753 to 130 ohm, R589 to 180 ohm.	
25		PWR	P56	De-rating thermal issue	Change PC41,42,43 to 62011HS00-015-G	
26			P64	Design Changed	Change H20 to new f/p pad_c50	
27			P24	Reduce noise	Change C417 and c420 to 0.uF	
28			P43	IEEE test fail.	Delete R745-R752	
29		EE	P43	Refer Intel guide rev 1.5	Add R768	
30			P32	Pin 42 of WWAN module is open drain .Add PU resistor at LED_WWAN_OUT# .	Add R767(100K ohm) and PU to "+3.3V_RUN_WWAN_PWR" for set"LED_WWAN_OUT#"	
31			P37	Modify Audio board pin define.	Modify Audio board pin define.	
32			P33	Change board ID.	Change board ID H493 to 8.2K.	
33			P33	Design Changed	Depop R456,R480,R462,U37	
34		PWR	P32-P60	Cost down	Change 0 ohm to short pad for power portion P52-P60.	
35			P56	Acoustic test result.	Change PC188,PC189 to 68uF(62110V000-024-G)	
36			P56	De-rating thermal issue	Change PC41,42,43 to 62010BL00-015-G	
37		EE	P37	P/N Changed	Change JAudio1 to GMS5P201-1203-BH and CN18 to H814021-0000-7H	
38			P11	Design Changed	Change R246 to 1K. modify GP1037 table.	
39			P33	P/N Changed	Change MEC5055 mfg PN to MEC5055-L2V-KR000 .	
40		PWR	P51	P/N Changed	Add PL1 Foxconn PN .	
41			P51	P/N Changed	Change PL1 part number to 1164AY-H-48/M=P3 and keep footprint.	
42			P46	Add pull down resistor R770 at TPM_B_DET#. Modified TPM selection table.	Add pull down resistor R770 at TPM_B_DET#. Modified TPM selection table.	
43			P33	Add MEC5055 Foxconn part number which the same in ST stage.	Add MEC5055 Foxconn part number which the same in ST stage.	
44			P07-P13	P/N Changed	Update PCH P/N to 21011K000-187-G	
45			P64	Add H27,H28	Add H27,H28	
46			P36	LED Current & Brightness adjust	Change LED RES R753,R588 to 390 ohm and R589 to 620 ohm	
47			P07-P13	P/N Changed	Update PCH P/N to 21011K000-187-G	
48			P04	P/N Changed	Change C249 part number to 622203J00-022-G because part number is error .	
49			P30,P37	EMI Request	Reserve R771,C557 for "CLK_DEBUG" and R772,C558 for "CLK_PCI_O2"	
50			P11	Intel feedback	Pop R196 for Intel ME setting.	
51			P07	HDMI Hot plug detect issue	Add C559 (620103600-011-G) to fix	
52			P56	Solve overshoot issue	Change PC69 and PC196 to 620105C00-026-G	
53						
54						
55						
56						
57						

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Ext Right Side Top)
	1	JUSB1 (Ext Right Side Bottom)
	2	JESA1 (Ext Left Side Top)
	3	JESA1 (Ext Left Side Bottom)
	4	WLAN/WIMAX
	5	MUX: Intel port to WWAN or Blacktop port to WWAN
	6	Bluetooth
	7	USH2-Host port
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Camera1/Camera2
	12	
	13	Mini CARD3

PM TABLE

	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW_PCH	+3.3V_SUS +1.5V_ME M	+5V_RUN +1.5V_RUN +1.8V_RUN +3.3V_RUN +0.75V_DDR_VT T +VCC_CORE +1.05V_RUN_VT	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

	USB PORT#	DESTINATION
USH	0	BIO
	1	None

SATA	DESTINATION		DIFFERENTIAL	DESTINATION	PCI EXPRESS	DESTINATION
SATA0	HDD		CLKOUT_PCIE0	MINI CARD-1 WWAN	Lane1	MINI CARD-1 WWAN
SATA1	ODD		CLKOUT_PCIE1	10/100/1G LAN	Lane2	MINI CARD-2 WLAN
SATA2	MINI CARD		CLKOUT_PCIE2	PCMCIA	Lane3	CARD READER
SATA3	None		CLKOUT_PCIE3	MiniWPAN (Mini Card 3)	Lane4	EXPRESS CARD
SATA4	ESATA		CLKOUT_PCIE4	EXPRESS CARD	Lane5	MINI CARD-3 PCIE
SATA5	DOCK		CLKOUT_PCIE5	MINI CARD-2 WLAN	Lane6	USB3.0
			CLKOUT_PCIE6	None	Lane7	
			CLKOUT_PCIE7	USB3.0	Lane8	PCMCIA
			CLKOUT_PEG8	CARD READER		
			CLKOUTFLEX0	SIO_14M		
			CLKOUTFLEX1	PCI_TCM		
			CLKOUTFLEX2	PCI_TPM		
			CLKOUTFLEX3	JETWAY_14M		